

PCB Layout Guidelines

This section provides PCB layout guidelines for Silanna’s Active-Clamp Flyback (ACF) Controllers. Careful layout considerations are important to optimize the performance of these devices.

There are two major current loops in an isolated AC-DC power supplies, shown in Figure 1, which need to be minimized for optimal performances, such as EMI and Efficiency. First, the primary side current loop which includes bulk capacitor, transformer primary winding, primary FET and primary sense resistor. Second, the secondary side current loop, consisting of transformer secondary winding, output capacitor and synchronous rectifier FET.

Several components for careful layout considerations are circled (red dotted) in Figure 1, marked from 1 through 7. The layout example provided in Figure 2 identifies these components and their recommended placements on the PCB.

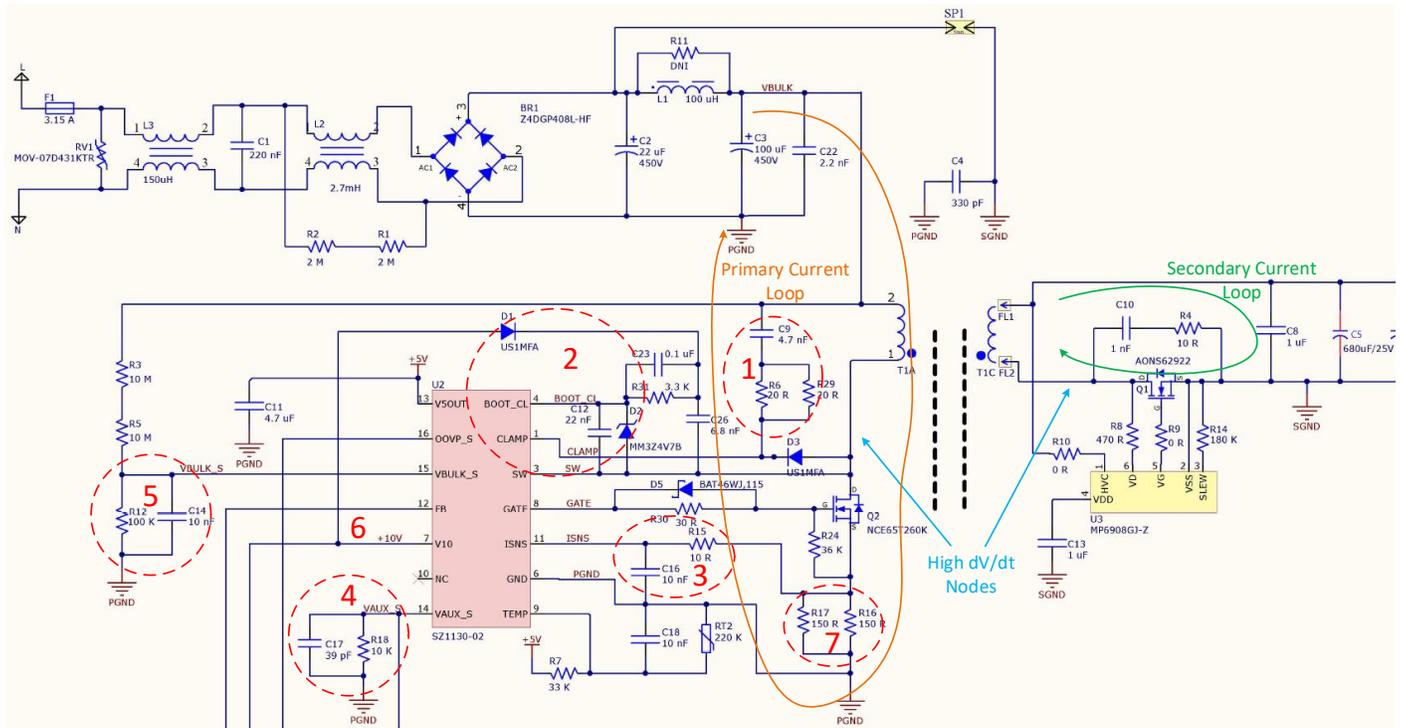


Figure 1: Schematic showing components for PCB layout considerations

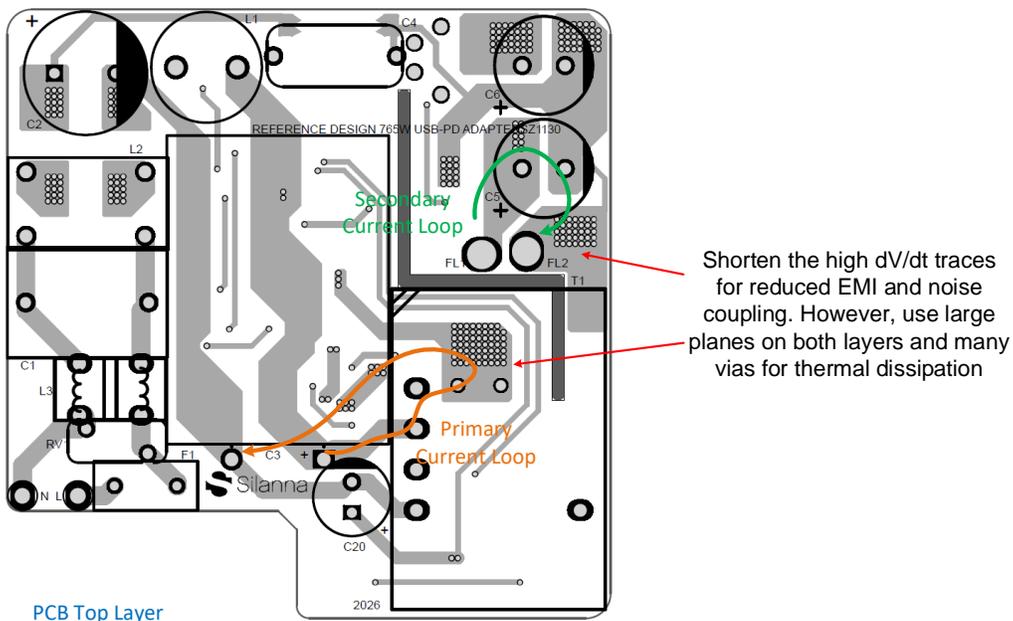
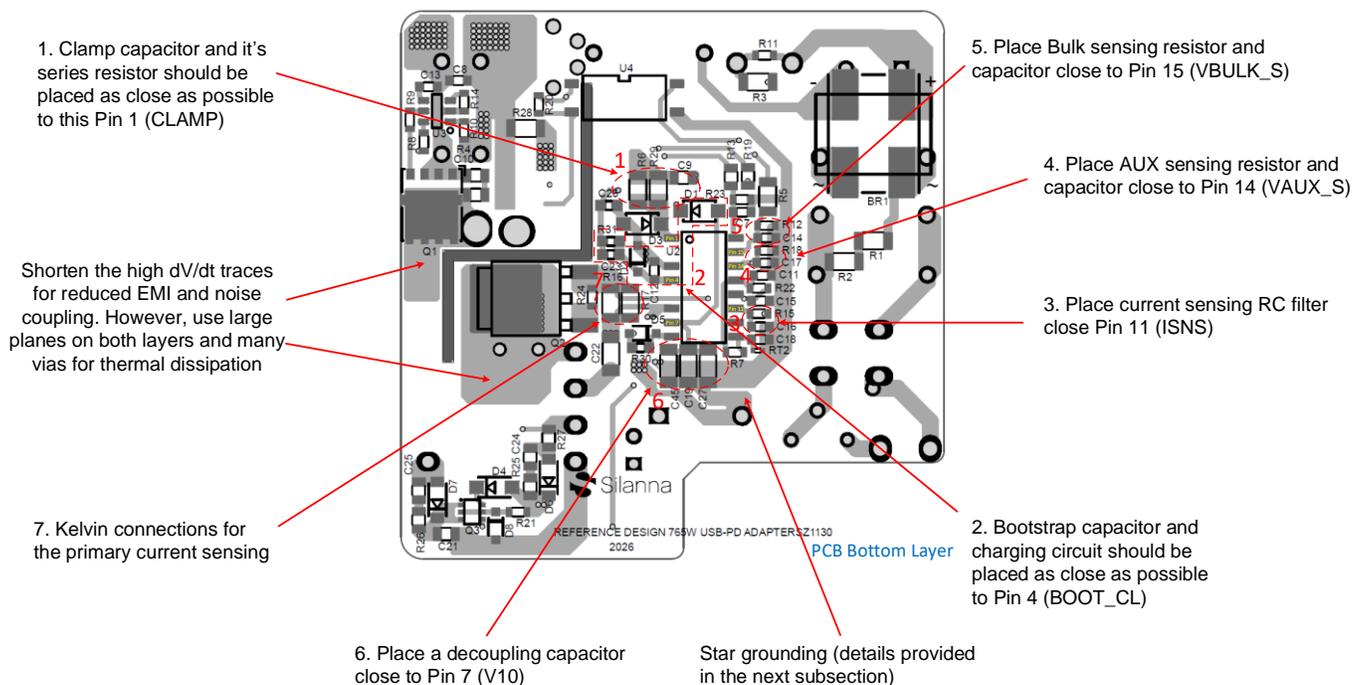


Figure 2: PCB layout example

Star Grounding

Proper ground connections are important for noise immunity, system stability and optimal performance of the power supply. Figure 3 below shows how a star grounding should be utilized in Silanna’s ACF based designs.

- Pin 6 (GND) and the sensing components for the low voltage pins (pull-down resistors of the voltage dividers, decoupling capacitors etc.) are connected to the negative terminal of V10 capacitor
 - V10 capacitor (C_{V10}) should be placed as close as possible to the IC
- The following circuit components are star grounded to the negative terminal of the input bulk capacitor
 - Negative terminal of the V10 capacitor
 - Power ground from the auxiliary bias circuit
 - Power ground of the primary current loop from sense resistor (R_{sense})
 - Optional Y-capacitor (if it needs to be connected to the primary ground)

Furthermore, Figure 3 shows how the Kelvin connections from the sense resistor, R_{sense} to the ISNS (Pin 11) RC filter and negative terminal of V10 capacitor (C_{V10}) are made (red lines).

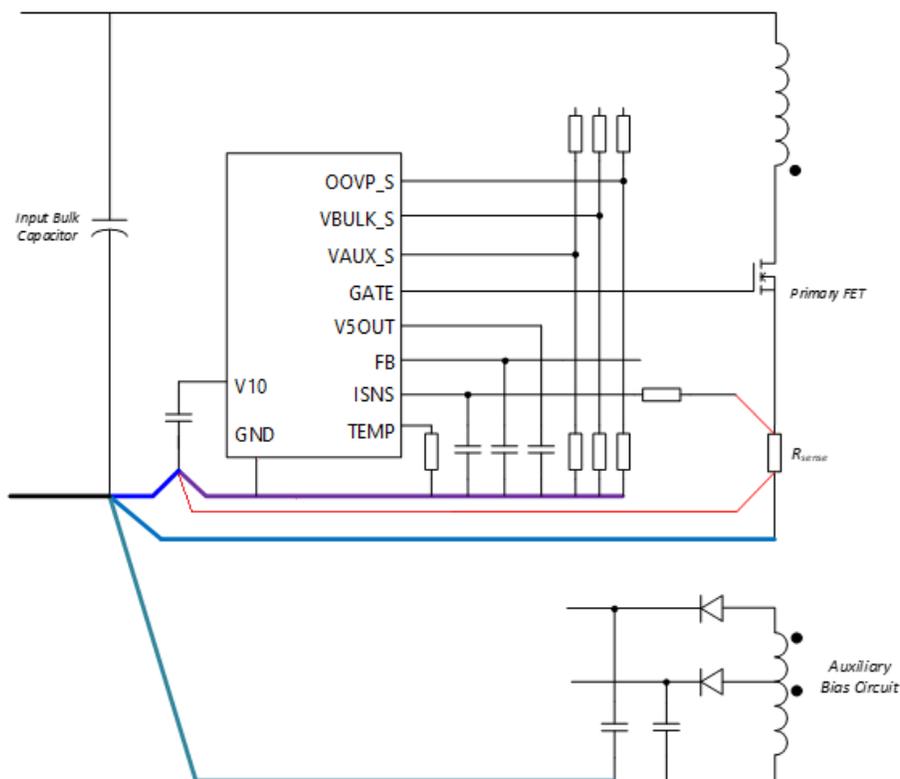


Figure 3: Star grounding of different circuit components