65 W Active Clamp Flyback

Application note AN1130 describes how to utilize Silanna's primary-side controller SZ1130 to design 65W high power density active clamp flyback converters for USB-PD applications.

Introduction

The SZ1130 is an Active clamp Flyback (ACF) PWM Controller that integrates an adaptive digital PWM controller and the following Ultra High-Voltage (UHV) components: active clamp FET, active clamp driver and a start-up regulator.

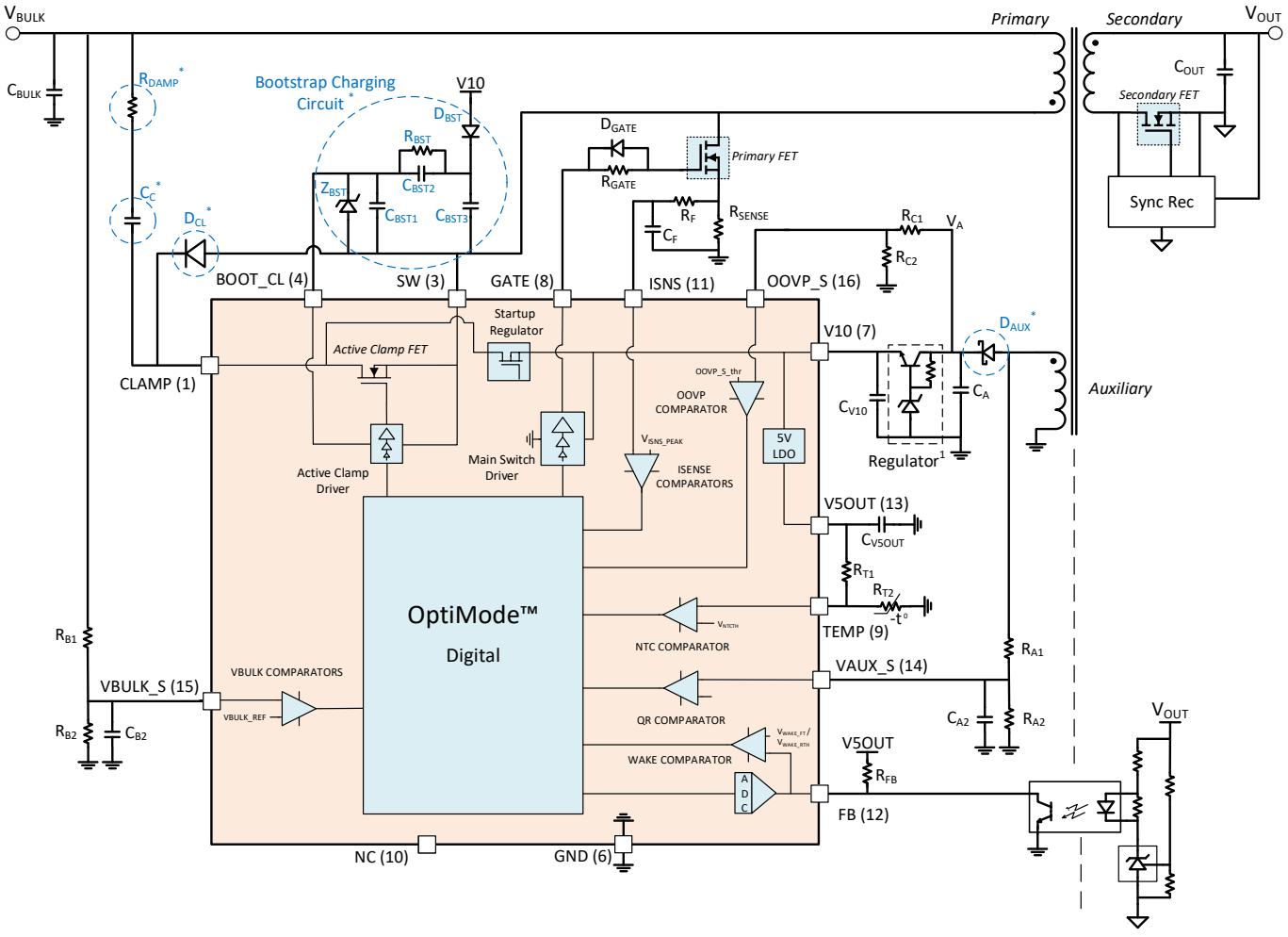

Figure 1: Typical Application Circuit of an Active clamp Flyback Converter using SZ1130

The device provides ease-of-design of a simple flyback controller with all the benefits of an ACF design, including recycling of the flyback transformer leakage energy and clamping of the primary FET drain voltage. Employing Silanna's OptiMode™ digital control architecture, the SZ1130 adjusts the device's mode of operation on a cycle-by-cycle basis to maintain high efficiency, low EMI, and fast dynamic load regulation.

Unlike conventional ACF designs, tight tolerances of the clamp capacitor and leakage inductance values are not required for proper operation of the circuit. Moreover, a small 3.3nF clamp capacitor is sufficient to realize the benefits of ACF operation. The SZ1130 is well suited for high efficiency and high-power density AC/DC power adapters. The device is designed for up to 65 W output power, including USB PD and Quick Charge applications.

Parameter	Min.	Typ.	Max	Unit
Input Parameters				
Line Voltage	90	-	264	Vrms
Line Frequency	47	60	63	Hz
Output Parameters				
Max output voltage		20		V
Min output voltage		5		V
Max output Power		65		W
Max output current		3.25		A
Over Current Limit		120		%

Table 1: Converter specification data

Design Procedure

Transformer design

This section provides detailed step by step procedure for designing a flyback converter. A 65W USB-PD (5-20V) charger has been selected as a design example.

Step 1: Estimate the input power

Assuming 20% over-current limit (OCL) allowance the maximum output power will be

$$P_{out}^{max} = P_{out} \cdot OCL$$

and the maximum input power as seen at the bulk capacitor is,

$$P_{in}^{max} = \frac{P_{out}^{max}}{\eta^{bulk}}$$

where η^{bulk} is the minimum efficiency of the converter from the bulk capacitor to the output capacitor, typically 94%.

Design Example

The maximum output power is obtained using equation 1:

$$\mathrm{P_{out}^{max}} = 65 \cdot 1.2 = 78\mathrm{W}$$

The maximum input power is obtained using equation 2:

$$\mathrm{P_{in}^{max}} = \frac{78\mathrm{W}}{0.94} = 83\mathrm{W}$$

Step 2: Determine the input bulk capacitance value

For universal AC line applications, bulk capacitance values equal to ~1.5uF per watt of input power are recommended in order to maximize efficiency and provide sufficient stored energy for continuous operation during IEC-61000-4-11 type voltage sag events. For applications where low AC line operation requirements are relaxed (either in terms of maximum output power, efficiency or voltage sag ride-through), the bulk capacitance values can be minimized.

For universal AC line applications, the recommended bulk capacitance value is

$$C_{bulk} = 1.5 \cdot P_{in}^{max}$$

If the above recommendation is not followed it is imperative that the capacitance value be chosen such that the minimum bulk voltage, v_{bulk_min}, is greater than SZ1130 brown-out threshold (recommendation 70V).

$$C_{bulk} > \frac{P_{in}^{max} \cdot (1 - D_{ch})}{f_{ac}} \cdot \frac{1}{2v_{ac\_min}^2 - v_{bulk\_min}^2}$$

where, v_{bulk_min} is the minimum input line voltage, P_{in}^{max} is the maximum input power, D_{ch} is the bulk capacitor charging duty ratio defined as shown in Figure 2, C_{bulk} is the bulk capacitance, f_{ac} is the minimum AC line frequency.

The charging duty ratio, Dch can be calculated as

$$D_{ch} = \frac{\frac{1}{4f_{ac}} - \frac{\sin^{-1}\left(\frac{v_{bulk\_min}}{\sqrt{2}\,v_{ac\_min}}\right)}{2\pi f_{ac}}}{\frac{1}{2f_{ac}}}$$

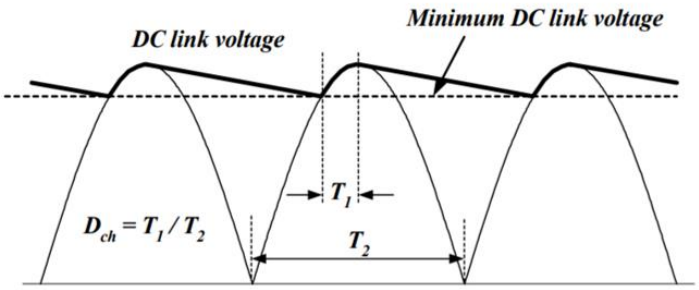

Figure 2: Input bulk capacitor voltage waveform

Design Example - C_{bulk} calculation

Assuming converter specifications outlined in Table 1, Dch & C_{Bulk} can be calcualted using the above equations:

$$D_{ch} = \frac{\frac{1}{4fac} - \frac{\sin^{-1}\left(\frac{v_{bulk\_min}}{\sqrt{2}\,v_{ac\_min}}\right)}{2\pi fac}}{\frac{1}{2fac}} = \frac{\frac{1}{4 \cdot 47} - \frac{\sin^{-1}\left(\frac{70}{\sqrt{2} \cdot 70}\right)}{2\pi \cdot 47}}{\frac{1}{2 \cdot 47}} = 0.315$$

$$C_{bulk} > \frac{P_{in}^{max} \cdot (1 - D_{ch})}{fac} \cdot \frac{1}{2v_{ac\_min}^2 - v_{bulk\_min}^2}$$

$$C_{bulk} > \frac{83 \cdot 0.685}{47} \cdot \frac{1}{2 \cdot 90^2 - 70^2} = 107uF \approx 120\text{uF (standard value)}$$

Step 3: Calculating primary-to-secondary turns ratio and primary magnetizing inductance

When the primary FET is off and the secondary side switch is conducting, the secondary side winding voltage is reflected on the primary winding. During this period, the primary FET drain and SZ1130 SW pin, V_{SW}, is exposed

to a voltage approximately equal to reflected secondary winding voltage (VVOR) plus the maximum bulk voltage (V_{bulk}). In order to ensure reliable operation of SZ1130 it is recommended that the maximum reflected secondary winding voltage, specifically the primary to secondary side transformer turns ratio, be selected in such a way that the primary FET peak drain and SW pin voltages are kept below 90% of the SZ1130 SW node maximum voltage rating, 620V.

The primary magnetizing inductance (L_M) can be calculated using,

$$L_M < \frac{(D_{max} * V_{bulk\_min})^2}{2 \cdot P_{IN_{MAX}} \cdot PCL_{\Delta} \cdot f_{sw\_min}}$$

Where f_{sw_min} is the minimum converter switching frequency, PCL_{Δ} is the peak-current limit variation (1.14) and D_{max} is the maximum primary side MOSFET duty cycle.

Design Example

The maximum allowable voltage at the drain of the FET/SW pin is, (Toshiba TK290P65Y is used as an illustration for the App note)

$$V_{SW} = V_{SW}^{max} \cdot 0.9 = 620V \cdot 0.9 = 558V$$

The maximum allowable reflected voltage, V_{VOR}^{max}, is given by the maximum allowable SW pin voltage and maximum bulk voltage ($1.1 \cdot V_{AC}^{max} \cdot \sqrt{2}$),

$$V_{VOR}^{max} = V_{SW} - V_{bulk}^{max} = 558V - (1.1 \cdot 265V_{RMS} \cdot 1.414) = 148V$$

The primary to secondary turns ratio can be calculated using the maximum allowable reflected voltage and maximum output voltage.

$$n = V_{VOR}^{max} / 1.05 \cdot V_{out}^{max}$$

$$n = 148V / 21V = 7$$

(Note: this is an approximation that does not take into account the clamp capacitor voltage ripple. The maximum primary side MOSFET drain-source voltage should be verified experimentally, or the design tool utilized to derive more accurate estimates)

During max duty-cycle operation it can be assumed that the flyback converter will be operating near boundary mode conduction and that the max duty cycle of the converter, D_{max}, is given by

$$D_{max} \approx V_{VOR} / (V_{bulk}^{min} + V_{VOR})$$

$$D_{max} \approx 140V / (70V + 140V) = 0.67$$

The minimum switching frequency is selected to be in the 30-40kHz range (lower frequency for optimized high-line efficiency and higher frequency for optimized low-line efficiency).

$$f_{sw\_min} = 40kHz$$

Substituting the values in the equation:

$$L_M < \frac{(0.67 \cdot 70)^2}{2 \cdot 83 \cdot 1.14 \cdot 40k} = 291uH$$

The selected value for Lm is 290uH.

Step 4: Core Selection and Primary Turns Calculation

The minimum number of primary turns (N_{P_min}) can be calculated using the formula

$$N_{P\_min} = \frac{L_M \cdot I_{max}}{B_{max} \cdot A_e} \cdot 10^6$$

where I_{max} is the maximum transformer primary current, A_e is the minimum equivalent magnetic core cross-sectional area in mm^2 and B_{max} is the saturation flux density in tesla (typically 0.3-0.34T).

Design Example (3C95 RM10)

Primary/Secondary Turns Calculation

$I_{max} = \frac{V_{bulk\_min} \cdot D_{max}}{L_m \cdot f_{sw\_min}}$ $I_{max} = \frac{70V \cdot 0.67}{290uH \cdot 40kHz} = 4A$

Note : With the 120uF Bulk cap , the new Vbulk_min is higher(~86V) but 70V is used in the calculation to account for any worst-case condition.

$$N_{P\_min} = \frac{L_m \cdot I_{max}}{B_{max} \cdot A_e} x\ 10^6$$

$$N_{P\_min} = \frac{290uH \cdot 4A}{0.33T \cdot 96\ mm^2}\ x\ 10^6$$

$$N_{P\_min} = 36\ T$$

$$N_S \geq \frac{N_{P\_min}}{n}$$

$$N_s \geq \frac{36}{7} = 5.1T$$

$$N_s = 5\ T$$

Step 5: R_{SNS} calculation and RC filter selection guide

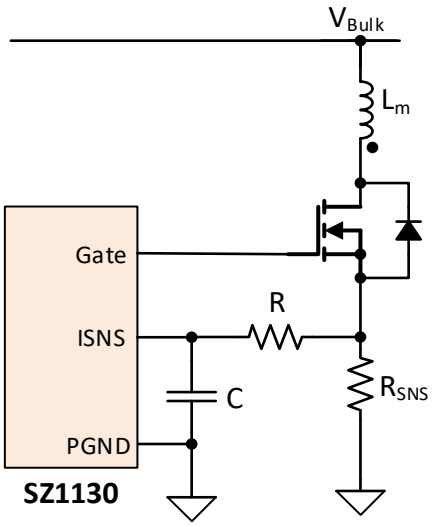

Figure 3: Rsense and RC filter circuit

SZ1130 implements two different ISNS thresholds. The skip pulse current threshold (V_{ISNS_SKIP}) is enabled during the light load operating conditions to improve efficiency. The peak current limit threshold (V_{ISNS_PEAK}) protection is to ensure the transformer does not saturate beyond I_{max} value and also to implement over power protection (OPP).

The formula to calculate R_{SNS} is given by

$$R_{SNS} = \frac{V_{ISNS\_SKIP}}{I_{MAX}}$$

where PCL^{max} is the maximum peak-current limit, as defined in datasheet, equal to 285mV.

Design Example

$$R_{SNS} = \frac{285mV}{4A} = 71m\Omega$$

In order to mitigate the effects of leading-edge current sensing noise, SZ1130 implements digital blanking, minimum value 221ns, of the current sensing comparator outputs. The main motivation is to ensure that the skip-pulse current limit (~37.5-55mV) is enforced during light load mode of operation and that high-frequency noise does not cause reduced primary MOSFET on-time, which can negatively affect efficiency.

One example where additional RC filter between the R_{SNS} resistor and ISNS pin is necessary is shown in Figure 4.

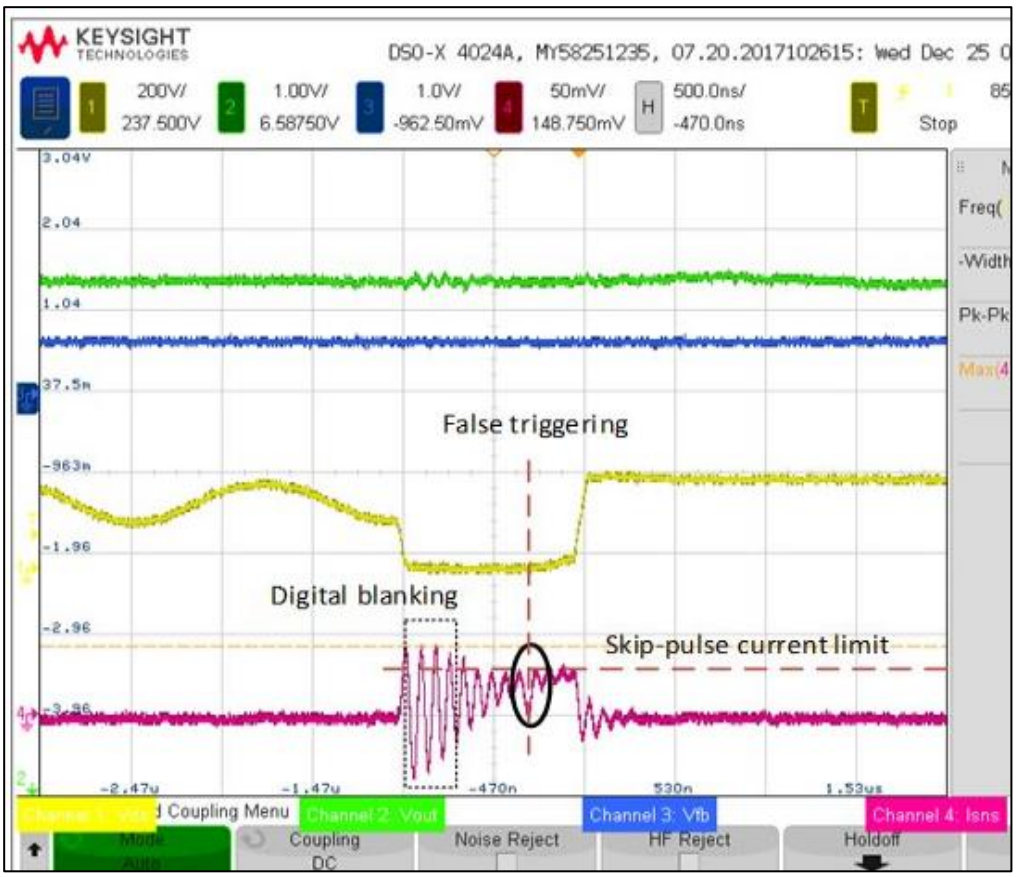

Figure 4: False triggering of skip-pulse current limit of due to high frequency noise

It should be noted that when a R_{SNS} RC filter is utilized it will result in higher skip-pulse and peak-current limits due to the added delay in detection. As a result, the peak-current limit value will increase by an amount equal to

$$i_{PCL}^{\Delta} = (1+\propto) \cdot \frac{BULK}{L_M} \cdot R \cdot C,$$

where α is given by

VBULK_S (DC)	α
<0.95V	0.75
≥0.95V, <1.7V	0.50
≥1.7V, < OVLO	0.375

Table 2: VBULK_S and corresponding α value

In order to maintain flat over-power protection, it is recommended that the RC filter be minimized to value less than 240ns (R = 10-24R and C = 10nF).

The skip-pulse current limit value will increase by an amount equal to

$$i_{SPL}^{\Delta} = \frac{BULK}{L_M} \cdot R \cdot C.$$

Note: In case of hard output short, the output voltage can be too low to support full discharging of the magnetizing current by the end of the switching period. This in turn will result in forced continuous conduction mode of

operation, where the primary MOSFET current which will be clamped to PCL current limit. As a result, the minimum SW node voltage can be in the 1-2V range when the primary MOSFET is on. Due to the minimum voltage at the SW node, the AC FET BOOT_CL may not be able to charge above the AC FET driver UVLO and AC FET will not be able to turn-on.

In such situation, it is recommended to minimize the RC filter to 6R/10nF in order to minimize the maximum CCM current and help ensure the AC FET can be engaged and SW node clamped.

Step 6: Gate resistor sizing

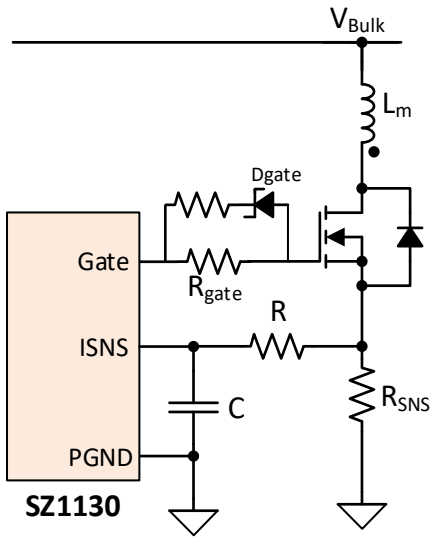

Figure 5: External gate resistor in series with the Main FET

An external series resistor may be needed in series with the gate of the primary FET to slow down the turn-on, reducing the falling dV/dt of the switching node (drain of the primary FET) voltage. Higher than 16 V/ns falling rate of switching node voltage can result in catastrophic failure of the device and hence, care must be taken when selecting R_{gate}. The minimum value of R_{gate} is provided by the following equation.

$$R_{gate} = \frac{V_{10} - V_{\text{Plateau}}}{C_{\text{gd}} \times \left| -\frac{dV_{sw}}{dt} \right|} - R_{gate\_pup}$$

where Cgd is the gate-to-drain capacitance (Crss from the FET datasheets) at drain-source voltage of 200V, |-dVSW/dt| is the absolute value of the maximum tolerable negative drain-source voltage when the primary MOSFET turns-on (16 V/ns), V10 is the typical V10 pin voltage (9.5V), VPlateau is the expected plateau voltage of the FET and R_{gate_pup} is the internal pull-up resistor (75 Ω typical).

A diode, D_{GATE} in parallel with R_{GATE} should be added to avoid any significant delay in turn-off time of primary FET due to the addition of R_{GATE}. A Schottky or fast recovery diode (trr ≤ 500 ns) is recommended for D_{GATE}.

Design Example

The MOSFET chosen for the app note is Toshiba TK290P65Y. The Rgate can then be calculated as:

$$R_{gate} = \frac{V_{10} - V_{\text{Plateau}}}{C_{\text{gd}} \times \left|-\frac{dV_{sw}}{dt}\right|} - R_{gate\_pup}$$
$$= \frac{10-6}{2.5p \times |-16\text{V/ns}|} - 75 = 25\ \Omega$$

Note:

Adding an external RGATE resistor introduces additional delay in turning-on the primary FET, reducing its effective on-time, depending on the value of the input capacitance (Ciss) of the FET. If an external RGATE is used, care must be taken to ensure bootstrap capacitor (CBST1) can be charged to ~2.5V after the completion of the very first primary FET gate pulse (~190 ns) is sent by SZ1130 during the startup. Detailed explanation on CBST1 sizing is provided in the active clamp gate-driver supply component selection section.

Step 7: Bias winding turns and bias capacitance calculation

The design of the two-level bias winding starts with establishing the number of bias turns required for sufficient bias capacitor and V10 voltage during no-load.

During no load operation the converter operates in burst mode, issuing at least 4 cycles per burst. While in burst mode, the V10 pin voltage must be maintained above 8.5V in order to guarantee that the internal UHV startup regulator remains off.

In order to calculate the required bias capacitor voltage and bias turns ratio, the burst repetition rate and the charge delivered per burst are required. Total charge delivered by 4 pulses is given by

$$Q_{burst\_4pulses} = 2 \cdot \left(I_{burst}^{peak}\right)^2 \cdot \frac{L_m}{V_{out}}$$

Where L_m is the transformer magnetizing inductance, V_{out} is the output voltage, and I_{burst}^{peak} is the peak primary FET current during burst mode.

$$I_{burst}^{peak} = \frac{50mV}{R_{SNS}}$$

The time between bursts can now be calculated.

$$t_{burst} = \frac{Q_{burst}^4}{i_{out}}$$

Where I_{out} is no load secondary current.

Using t_{burst} the top winding C_{aux} capacitance, can now be calculated.

$$C_{aux} = \frac{I_{ic} \cdot (t_{burst} - t_{V10})}{\Delta V_{aux}}$$

$$t_{V10} = \frac{C_{10} \cdot (V_{10}^{min} - 8.5)}{I_{ic}}$$

Where, V_{10}^{min} is the worst case minimum voltage that the dual-MOSFET regulator will generate over entire operating range.

The aux winding must provide 8.5V for IC operation and also compensate for regulator drop, diode voltage and Vaux ripple.

$$V_{aux} = 8.5V + \text{regulator drop} + \text{diode voltage drop} + \text{Vaux ripple}$$

$$N_{aux} \geq \left(\frac{N_{sec}}{V_{out\_min}}\right).V_{bias}$$

Design Example – Top Bias Winding turns and capacitance

Primary/Secondary Turns Calculation

$$I_{burst\_peak} = \frac{50mV}{0.076\Omega} = 0.658A$$

Four pulses of 0.746A will deliver a total charge equal to:

$$Q_{burst\_4pulses} = 2 \cdot (0.658\text{A})^2 \cdot \left(\frac{290uH}{5V}\right) = 5\ x\ 10^{-5}$$

The time between bursts can now be calculated, assuming no load secondary current of 1.4mA (in actual designs it will be dependent on PD controller that is used and feedback network).

$$t_{burst} = \frac{5\ x\ 10^{-5}C}{1.4\text{mA}} = 35.7ms$$

$$t_{V10} = \frac{47\mu F \cdot (9\text{V} - 8.5V)}{1.4mA} = 16.7ms$$

Using t_{burst} ,V10 input supply no-load current 2.9mA (datasheet) and assuming 5V as Vaux ripple the C_{aux} capactior can now be calculated

$$C_{aux} = \frac{2.9mA \cdot (35.7ms - 16.7ms)}{5\text{V}} = 11\mu\text{F} \rightarrow 12\text{uF (standard value)}$$

Calculating N_{bias} must provide 8.5V for IC operation, ~1.2V for regulator drop, 0.4V for diode voltage, and 5V to compensate for V_{aux} ripple. Therefore the winding must produce:

$$V_{aux} = 8.5V + 1.2V + 0.4V + 5V = 14.1$$

$$N_{aux} \geq \left(\frac{N_{sec}}{V_{out\_min}}\right) \cdot V_{aux} \geq \frac{5T}{5V} \cdot 14.1\text{V} = 14.1\text{T}$$

Use 14T for N_{aux}.

Design Example – Bottom Bias Winding turns and capacitance

To calculate the bottom bias winding tap position, the output voltage at which the tap becomes active must be selected. This selection can be based on desired efficiency optimization and/or dual auxiliary component voltage ratings, in this example the maximum output voltage is selected.

To provide the minimum V_{bias} voltage at 15V output voltage, the bias winding tap must provide 8.5V for IC operation, ~1.2V for regulator drop, 0.4V for diode voltage and 4V to compensate for the V_{aux} ripple

$$V_{bias} = 8.5V + 1.2V + 0.4 + 4 = 14.1$$

$$N_{tap} \geq \left(\frac{N_{sec}}{V_{out}}\right) \cdot V_{bias_{tap}} = \frac{5\,T}{15\,V} \cdot 14.1\text{V} \geq 4.7\text{T (5T)}$$

The bottom bias winding capacitance value is calculated such that it's discharge rate is slower than the bus capacitance discharge rate in case of output over voltage fault. This is required in order to ensure that when SZ1130 hiccups (restarts) there are no circulating currents from the output bus to the bias winding capacitors, which can cause large voltage spikes on the secondary side MOSFET.

$$C_{aux}^{bottom} \geq C_{bus} \cdot \frac{I_{V10}^{fault}}{I_{VOUT}^{OOVP}} = 1mF \cdot \frac{0.7mA}{7mA} = 100uF$$

It should be noted that most PD ICs support active discharging of the output bus node in case of output over voltage events. If such a feature exists it is highly desirable that it is enabled since it will significanlty reduce the required C_{aux}^{bottom}. An example is shown below where a 20mA discharge current is enabled during output over voltage event.

$$C_{aux}^{bottom} \geq C_{bus} \cdot \frac{I_{V10}^{fault}}{I_{VOUT}^{OOVP}} = 1mF \cdot \frac{0.7mA}{20mA} = 35uF$$

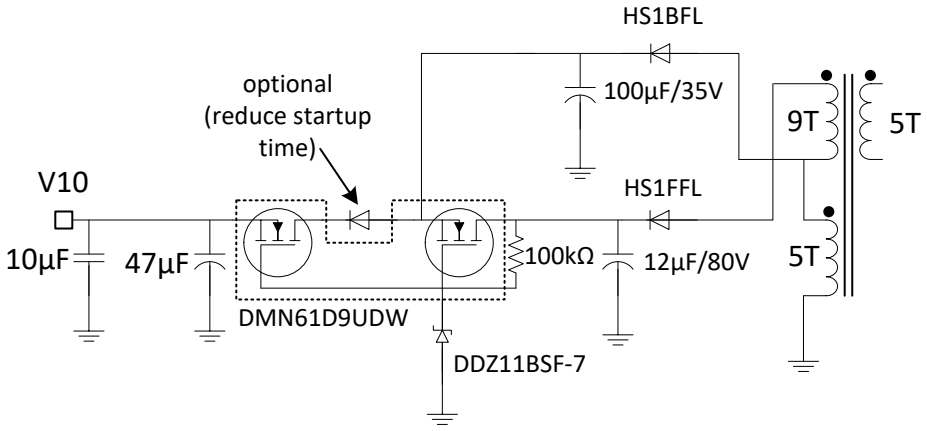

Figure 6: Dual-winding auxiliary regulator circuit for high performance USB PD applications

Step 8: Core gap

With the determined turns of the primary side, the gap length of the core is obtained as

$$l_g \approx \mu_0 \frac{N_{pri} \cdot I_{max}}{B_{max}} \cdot \text{mm}.$$

Design Example: Gap Calculation

As only a minimal amount of energy is stored in the core itself, this factor may be ignored to simplify calculation.

$$l_g = 4\pi \cdot 10^{-7} \cdot \frac{36\text{T} \cdot 4\text{A}}{0.33\text{T}} = 0.55mm$$

Step 9: Determine the wire diameter

The recommended bobbin for the design example is YT-1032 and the specifications are shown below:

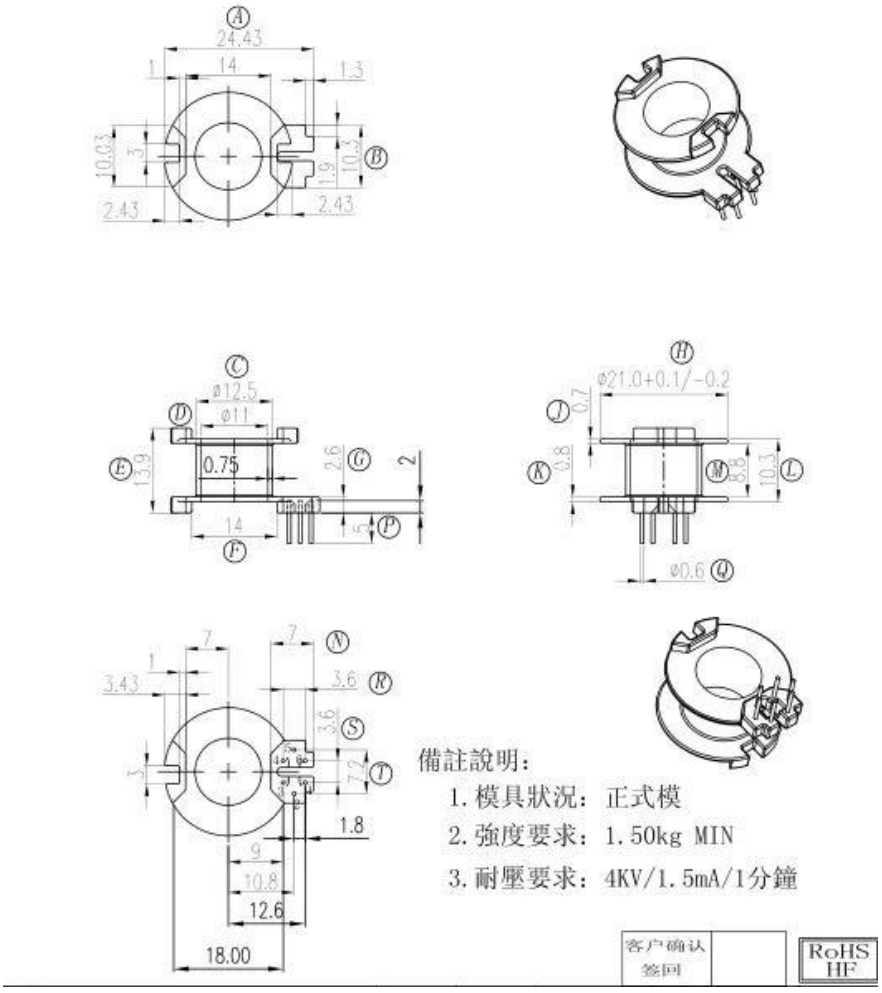

Figure 7: YT-1032 bobbin specifications

The objective is to determine the appropriate wire diameter & number of strands so that copper losses (DC & AC resistance) are minimized. The first step is to determine the primary winding diameter. The primary winding diameter is calculated based on the skin depth to minimize the AC loss.

For the primary magnetizing current, which is a triangular shaped waveform, the major harmonics are the 1st and the 3rd.

Skin depth for the 3rd harmonic can be calculated as, $\delta = \sqrt{\frac{\rho}{\pi .\mu o .\mu r .f}}$

Where,

ρ is the resistivity of the wire material (copper)

μo = permeability of free space

μr is the relative magnetic permeability of the wire material,

f is the frequency of interest.

$$\delta = \sqrt{\frac{2.3 * 10^{-8}}{\pi * 4\pi * 10^{-7} * 300k}} = 0.139mm$$

Assuming a fill factor of 90%, the maximum primary winding radius can be calculated as below:

$$\text{Fill factor} = \frac{(2 * primary\ winding\ \ radius) * \frac{N_p}{number\ of\ primary\ layers}}{Winding\_area\_length}$$

$$0.90 = \frac{(2 * primary\ winding\ \ radius) * \frac{36}{2}}{8.8}$$

Primary winding radius = 0.22 mm

Since the calculated skin depth δ is 0.139mm, the primary winding radius must be <0.139mm. Hence, two strands in parallel is required. So, the primary winding strand radius will be:

Primary winding radius = 0.22 / 2 = 0.11mm

The closest to that is AWG31 (0.113 mm).

Once the wire size is determined, it is a good practice to calculate the current capacity (circular mils per amp or CMA).

$$\text{Circular Mil per Amp , CMA} = \frac{CM\ of\ the\ winding * No\ of\ parallel\ winding}{Irms}$$

For a nominal operating condition, V_{ac} =90Vrms ,V_{out} =20V, I_{out} =3A and C_{bulk} = 120uF, L_m= 290uH, N_p =36T, N_s =5T. The calculated primary I_{rms} value is ~1.13A.

$$\text{Circular Mil per Amp, CMA} = \frac{79.7 * 2}{1.13} = 141.$$

The calculated CMA value is relatively lower than the nominal (200~500) range. This is the design trade-off to use RM10LP Core and Interleave winding structure. If the CMA value calculated is not acceptable then iteration is required to increase the CM of the winding which in turn may result in increasing the number of layers or choosing the next larger core size.

Secondary Winding

The secondary winding is usually a triple insulated wire i.e. it has three distinct layers of insulation, such that the insulation safety requirements between primary and secondary side is met. Like the primary, secondary current waveform is also triangular. Hence considering major harmonics 1st and 3rd, the calculated skin depth is 0.139mm.

$$\text{Secondary winding wire diameter} = \left(\frac{Winding\ area\ length\ *FF}{Ns}\right) = \frac{8.8 * 0.9}{5} = 1.584\text{mm (0.0623in)}$$

Since the calculated skin depth δ is 0.139mm, the constraint is that the strand OD has to be AWG31 or higher AWG. From the Table 3 below, TXXL230/44TXXX-3 (MWXX) can be selected since it is nominal OD is close to the theoretical calculations and meets the constraints.

PART NUMBER	EQUIV. AWG	CORE O.D. (in)	CIR. MILS	NO. STRANDS	AWG OF STRANDS	NOMINAL O.D.(in)
TXXL180/38TXXX-2(MWXX)	13.5	0.0694	2880	180	38	0.0814
TXXL180/38TXXX-3(MWXX)	13.5	0.0694	2880	180	38	0.0874
TXXL15/30TXXX-1.5(MWXX)	16.5	0.0485	1500	15	30	0.0575
TXXL15/30TXXX-2(MWXX)	16.5	0.0485	1500	15	30	0.0605
TXXL15/30TXXX-3(MWXX)	16.5	0.0485	1500	15	30	0.0665
TXXL360/44TXXX-2(MWXX)	15	0.0557	1440	360	44	0.0677
TXXL360/44TXXX-3(MWXX)	15	0.0557	1440	360	44	0.0737
TXXL19/36TXXX-2(MWXX)	21.5	0.0281	475	19	36	0.0401
TXXL19/36TXXX-3(MWXX)	21.5	0.0281	475	19	36	0.0461
TXXL35/38TXXX-2(MWXX)	21	0.0306	560	35	38	0.0426
TXXL35/38TXXX-3(MWXX)	21	0.0306	560	35	38	0.0486
TXXL07/30TXXX-1.5(MWXX)	20	0.0331	700	7	30	0.0421
TXXL07/30TXXX-2(MWXX)	20	0.0331	700	7	30	0.0451
TXXL230/44TXXX-2(MWXX)	17	0.0445	920	230	44	0.0565
TXXL230/44TXXX-3(MWXX)	17	0.0445	920	230	44	0.0625
TXXL40/40TXXX-1.5(MWXX)	22	0.0254	385	40	40	0.0344
TXXL40/40TXXX-2(MWXX)	22	0.0254	385	40	40	0.0374
TXXL07/32TXXX-1.5(MWXX)	21.5	0.0267	448	7	32	0.0357
TXXL07/32TXXX-2(MWXX)	21.5	0.0267	448	7	32	0.0387
TXXL19/40TXXX-1.5(MWXX)	25.5	0.0175	183	19	40	0.0265
TXXL19/40TXXX-2(MWXX)	25.5	0.0175	183	19	40	0.0295
TXXL05/32TXXX-1.5(MWXX)	23	0.0226	320	5	32	0.0316
TXXL05/32TXXX-2(MWXX)	23	0.0226	320	5	32	0.0346
TXXL16/44TXXX-1.5(MWXX)	30	0.0101	64	16	44	0.0191

Table 3: Wire Part Number and corresponding AWG & O.D value

Corresponding CMA value of the secondary winding can be calculated as:

$$\text{Circular Mil per Amp , CMA} = \frac{CM\ of\ the\ winding * No\ of\ parallel\ winding}{Irms}$$

From the Table 3, the equivalent CMA value for the TXXL230/44TXXX-2 (MWXX) wire is 920. For the same nominal operating condition (as used in the primary winding CMA), the secondary Irms current was calculated as ~ 5.83A.

Circular Mil per Amp, CMA = $\frac{920*1}{5.83}$ = 156

Auxiliary winding

For the auxiliary winding the recommended wire gauge is AWG 32 (0.202mm diameter), the number of layers is 1 and parallel wires is 1.

Step 10: Determine the active clamp external components

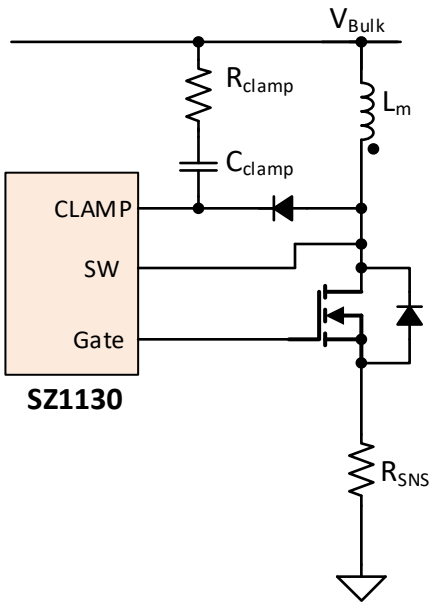

Figure 8: Clamp circuit consisting of active clamp capacitor, resistor and parallel diode.

The selection of the active clamp capacitor, C_{clamp}, is a two-step process. First, the initial estimation of C_{clamp} should be made based on the average transformer leakage inductance value, $L_{leakage}$, using the following equation.

$$C_{clamp} = \left(\frac{T_{RES}}{2\pi}\right)^2 \cdot \frac{1}{L_{leakage}}$$

Where, T_{RES} is the resonant period of C_{clamp} and $L_{leakage}$, which should be set to 1µs. If $L_{leakage}$ is unknown, a reasonable estimate would be 1.5% of the primary side magnetizing inductance.

Second, check T_{RES} during full-power operation, at maximum output voltage, and adjust C_{clamp} to ensure 0.9-1µs resonant period is achieved. Figure 9 identifies this resonant period from the drain voltage waveform of the primary FET after it turns off

Figure 9: Typical primary MOSFET drain voltage and active clamp current with the active clamp resonant period highlighted

The voltage rating of C_{clamp} needs to be calculated to withstand the DC component of reflected output voltage and the AC component of ΔVC_{Clamp}:

$$V_{MIN\_C_C} = V_{OUT\_MAX} \cdot \frac{N_{PRI}}{N_{SEC}} + \Delta V_{C_C}$$

where the AC component ΔVCC, is given by:

$$\Delta V_{C_C} \approx \frac{\pi}{4} \cdot Imax \cdot \sqrt{\frac{L_{LK}}{C_C}}$$

$$= \frac{\pi}{4} \cdot \frac{V_{ISNS\_PEAK}}{R_{SENSE}} \cdot \sqrt{\frac{L_{LK}}{C_C}}$$

Design example

For the primary magnetizing inductance of 290uH, considering leakage inductance to be ~1.5% and setting the resonant period as 1us.

Leakage inductance = 1.5% L_M = 4.35µH

Capacitor clamp,

$$C_{clamp} = \left(\frac{1.10^{-6}}{2\pi}\right)^2 \cdot \frac{1}{4.35 * 10^{-6}.} = 5.82\text{nF}$$

the AC component ΔVCC,

$$\Delta V_{C_C} = \frac{\pi \cdot 290m}{4 \cdot 76\text{m}} \cdot \sqrt{\frac{4\text{u}}{5.82\text{n}}} = 78.56V$$

Minimum voltage rating of the capacitor,

$$V_{MIN\_C_C} = 20 \cdot \frac{40}{6} + 78.56 = 211.89\text{V (250V)}$$

Clamp resistor

The optimal point to turn-on the AC FET is when active clamp current is flowing through the AC FET body diode (ZVS) and optimal point to turn-off is when active clamp current is close to zero (ZCS) or the AC FET body diode is conducting (ZVS). If the variation of the leakage inductance and clamp capacitor value (ex. C0G) can be controlled within 0.7-1.4x of nominal value a series clamp resistor is not required (ZVS will be achieved during turn on and turn off).

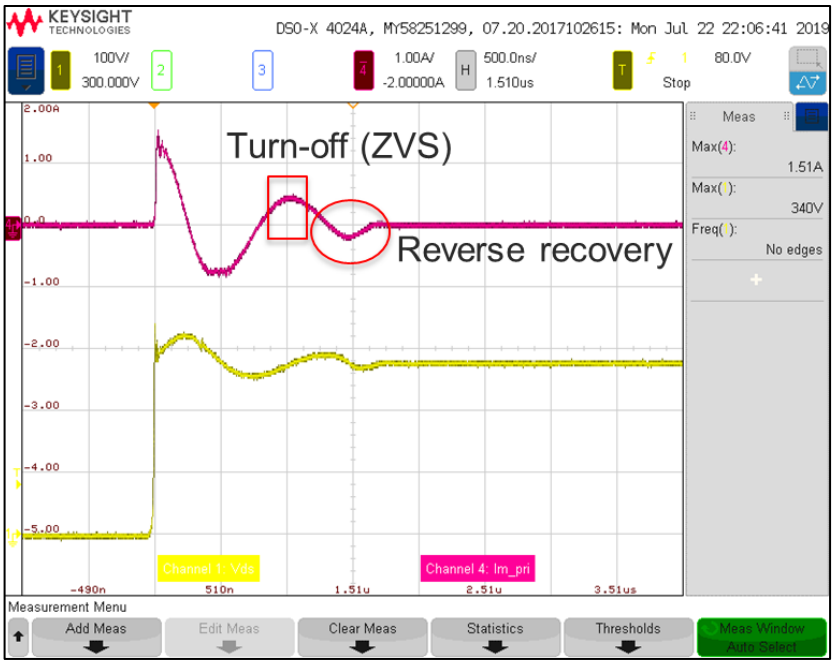

Figure 10: 115Vac/20V/3A w/o clamp resistor. CH1 is the primary MOSFET drain voltage and CH4 is the active clamp current (positive from source-to-drain).

If the leakage inductance cannot be well controlled (within 0.7-1.4x), it is recommended to add a clamp resistor in series, typically 10R-20R (10R 1812 footprint, 20R 2512), in order to ensure the AC FET turn-off is soft-switched (ZCS). Figure 10 illustrates the active clamp current without a clamp resistor (ZVS turn-on and turn-off) and Figure 11 illustrates the active clamp current with a 20R clamp resistor (ZVS turn-on and ZCS turn-off).

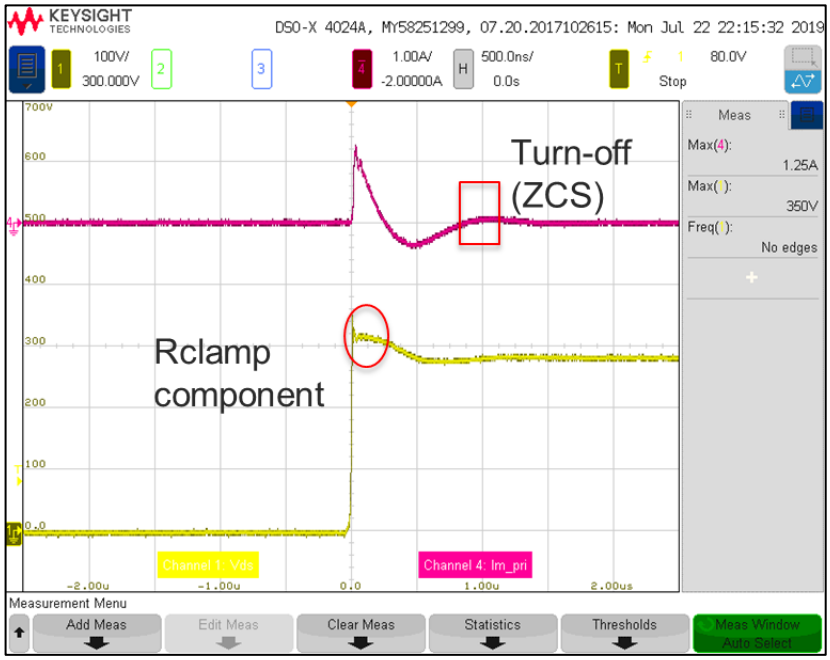

Figure 11: 115Vac/20V/3A w/ 23R clamp resistor. CH1 is the primary MOSFET drain voltage and CH4 is the active-clamp current (positive from source-to-drain).

Active clamp FET parallel diode

An external parallel diode is required in the circuit to prevent the AC FET damage during single point failure periods when start-up regulator can be on, drawing up to 11mA of current through the body diode, and the primary MOSFET turn-on events with large negative primary drain dv/dt slew-rate, -10V/ns.

Parameter	Value
Max DC reverse voltage	≥ 800V
Average rectified current	≥ 1 A
Reverse recovery time (trr)	≤ 75ns
VF @ 10mA	<= 0.6V
Recommended parts	US1MFA, HS1KFL

Table 4: Clamp diode selection criteria

Step 11: Determine the active clamp gate-driver supply bootstrap components

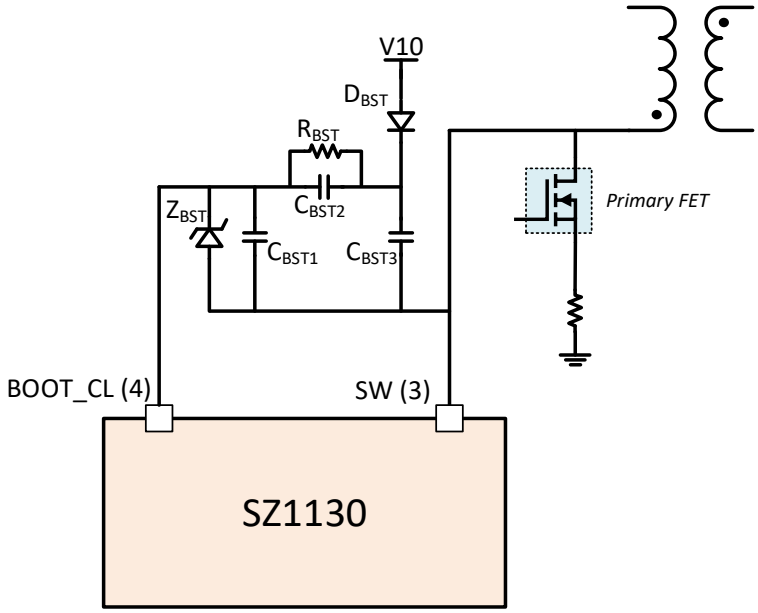

Figure 12: Bootstrap capacitor circuit

The voltage supply to the internal AC FET high side driver is provided by the C_{BST1} connected between the BOOT_CL & SW pin. To ensure that ACFET is active after the startup, the C_{BST1} must be sufficiently charged above ACFET driver UVLO (~3.6V typical). An enhanced BOOT_CL charging circuit is implemented which comprises of C_{BST3}, a capacitor divider (C_{BST2}, C_{BST1}) and a Zener diode, to regulate the voltage between BOOT_CL and SW.

The enhanced charging circuit has two objectives -First, the peak overshoot due to the inrush current during the first pulse should be below Max BOOT_CL voltage rating (5.5V) and second, is to charge the C_{BST1} to above 0.5V during the first pulse. The selection of the capacitor divider value is based on the experimental observation. For example, if the C_{BST3} between SW and D_{BST} is charged to ~6v during the 1st pulse in room temp with 30Ω R_{gate}, then the capacitor divider of 22nF(C_{BST1}) and 100nF(C_{BST2}) would charge BOOT_CL to ~2.7V as shown in Figure 12 . Over the time, when C_{BST3} is charged to a higher value, the Zener diode would clamp the voltage across the C_{BST1} to a safe range for ACFET gate driver.

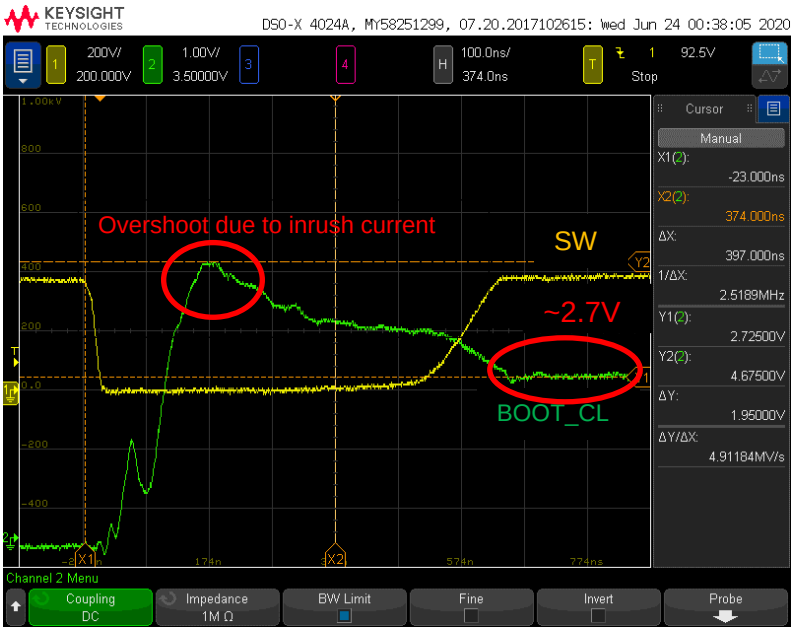

Figure 13: BOOT_CL voltage charged to ~2.7 during the first pulse

It should also be noted that CBST needs to be sized to limit the worst-case steady state ripple to ~100 mV. To limit the voltage ripple within 100 mV, CBST needs to be larger than 10 nF.

Design example

The recommended values

Parameter	Value
C_{BST1}	22nF (50V, X7R)
Z_{BST}	MM3Z4V7B
CBST2	100nF
CBST3	6.8nF
R_{BST}	US1MFA, HS1KFL
D_{BST}	US1MFA

Step 12: Capacitor Sizing

V10 is the SZ1130 supply voltage input (8.5 V -10.5 V) that provides power to the internal circuits, including the primary FET gate driver, the 5 V LDO and the bootstrap circuit for the internal Active Clamp FET driver. The V10 should always be above the falling POR threshold of 8.3V typical. It is recommended to use a large cap at first, typical recommendation is 47uF e-capacitor and 10uF ceramic capacitor. The selection of the optimal V10 cap value is based on the experimental observation.

For example , the Figure 14 is the start-up at 90Vac and -40℃ ambient temperature with recommended 47uF e-cap and 10uF ceramic capacitor. The V10 voltage is above 8.5V before Aux winding takes over.

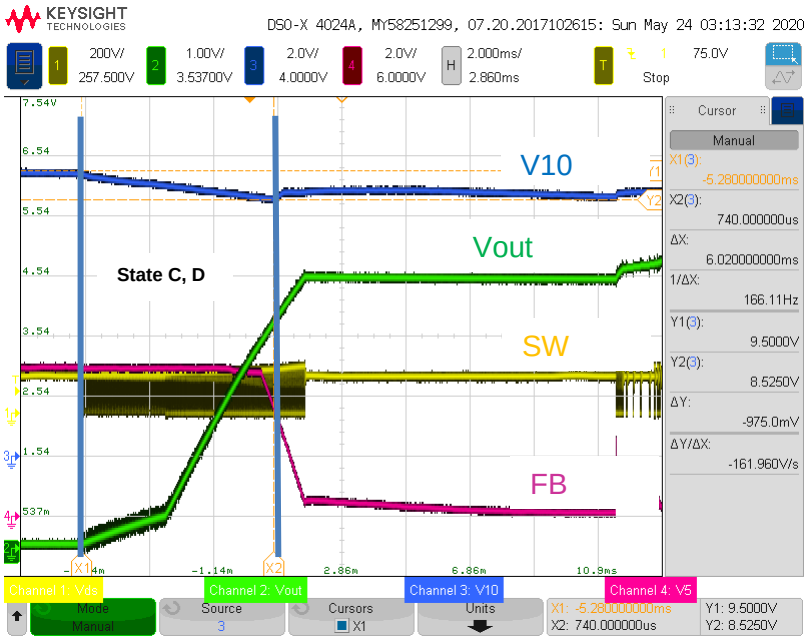

Figure 14: **V10 voltage waveform during the start-up**

The time needed for the Aux winding to take over from the start-up LDO depends how fast output voltage rises and turns ratio between aux and secondary (State C, D).If the time taken by the aux regulator to take over is assumed to be independent of V10 cap value, the theoretical capacitance value can then be calculated by the following equation:

$$C_1 = C_2 * \frac{dv_2}{dv_1}$$

where $C_1$is the design value, $C_2$is the initial value , $dv_2$is target voltage drop, $dv_1$is the voltage drop with initial V10 value. In case, a user chooses to set the minimum V10 voltage to a different value say 9V, then the new V10 capacitance value can be calculated as.

$$\mathrm{C1} = 57uF * \frac{9.5-8.5}{9.5-9} = 114\mathrm{uF}$$

Note: To account for IC variations like IC current consumption, V10 capacitance, and QR detection sensitivity, it is recommended to provide some margin on minimum V10 voltage. Hence, it is advised to set the voltage >8.5V.

Step 13: Auxiliary regulator circuit

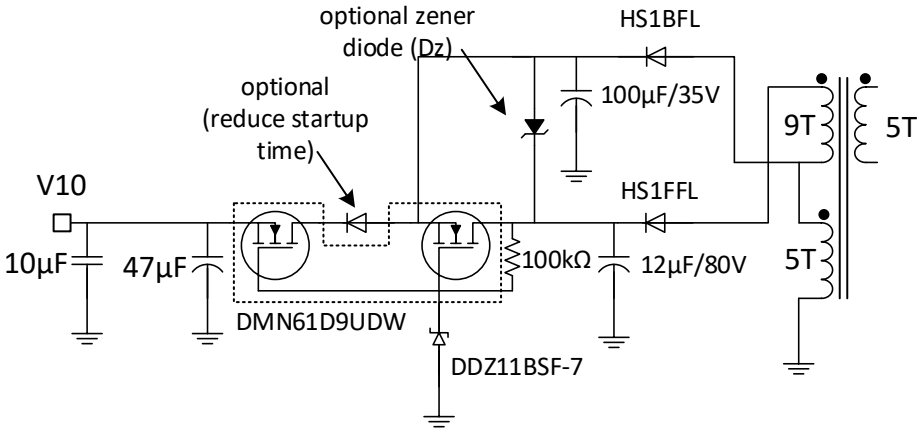

Figure 15: Dual-winding auxiliary regulator circuit for high performance USB PD applications

During startup, an integrated UHV start-up regulator provides power to Pin 7 (V10), until the more power efficient auxiliary winding takes over. For applications where the output voltage may vary over a wide range, such as USB-PD or Quick Charge, the reflected rectified auxiliary winding voltage will be outside of the acceptable 8.5 V - 10.5 V V10 pin voltage range. As a result, a discrete external regulator will be required to provide regulated power to V10 from the rectified AUX winding node. In such applications, where the output voltage may vary from 5 to 20 V a dual-auxiliary winding and dual MOSFET external regulator, as shown in Figure 15, is recommended in order to minimize SZ1130 power losses during maximum output voltage operation.

It should be noted that the external regulator component voltage ratings should be based on the maximum positive and negative reflected voltage on the AUX winding as given below equation. This requirement must be considered for both steady state and transient, including fault conditions.

$$V_{AUX}^{MAX} = \left(V_{OUT\_MAX} \cdot \frac{N_{AUX}}{N_{SEC}}\right)$$

$$V_{AUX}^{MIN} = -\left(V_{BULK\_MAX} \cdot \frac{N_{AUX}}{N_{PRI}}\right)$$

Note:

The LDO MOSFET's should be selected based on the maximum VCC1, VCC2 voltages measured on the bench. The typical VDS rating of the dual LDO MOSFET's used in a 20V,65W application is 60V. Theoretically, the max voltage on the AUX_ should be ~53V from the above equation. But, due to the leakage inductance, the AUX capacitors see higher voltage than the theoretical value. the max voltage on the AUX is observed to be ~85V.Hence, the voltage across one of the MOSFET which is equal to difference between VCC1, VCC2 is ~60V, which is the Vds breakdown voltage.

Over-voltage Fault:

In case of output over voltage fault, the voltage difference between VCC1 and VCC2 can be considerably higher compared to the steady state before the fault is detected. Hence, the values of VCC1 and VCC2 capacitors and the voltage rating of MOSFET pair must be considered taking this into account.

For an example, during the USB-PD FB to SGND short, if VCC2 discharges faster than VCC1 then the dual MOSFET could potentially see more than the rated VDS voltage. Hence, the bottom bias winding capacitance value (in Step 7) is calculated such that it's discharge rate is slower than the bus capacitance discharge rate in case of output over voltage fault Figure 16 is the waveform captured during the output OVLO fault with the calculated VCC2 capacitance value (100uF). The maximum value of the VCC1-VCC2 voltage observed is ~55V, which is within the safe operating area of the LDO MOSFET. An optional 56V Zener (Dz) can be added between VCC1 and VCC2 for additional protection.

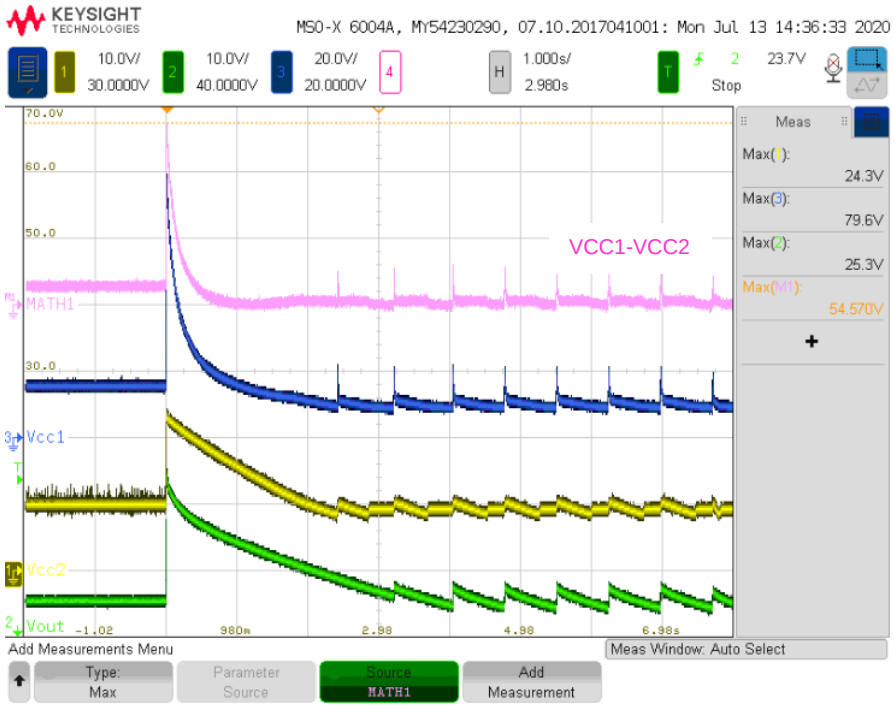

Figure 16: **VCC1, VCC2 waveforms captured during the over voltage fault.**

Step 14: BULK_S sensing resistors

The under-voltage/brown-out/brown-in are implemented using bulk capacitor voltage sensing with a resistor divider connected to VBULK_S.

Universal line voltage range (82 Vac to 300 Vac)

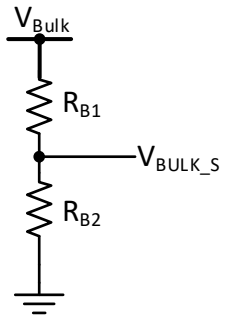

Figure 17: Simple bulk voltage sensing circuit

A basic resistor divider, as shown in Figure 17, can be utilized to ensure operation over universal line voltage range with margin. To minimize the no-load power a large R_{B1} resistance value, 4x22MΩ, is recommended.

The BULK_S pull-down resistance should be calculated taking into account the desired maximum brown-in voltage ($V_{AC}^{brown-in}$), the BULK_S brown-in threshold V_{UV_REC} (0.655V), and the desired RB1 resistance value. Both R_{B1} & R_{B2} are recommended to be within 1% tolerance.

$$R_{B2} = \frac{R_{B1}}{\left(\frac{V_{BULK}^{brown-in}}{V_{UV\_REC}} - 1\right)} = \frac{88M\Omega}{\frac{V_{AC}^{brown-in} \cdot \sqrt{2}}{0.575V} - 1}$$

Once R_{B1} and R_{B2} are calculated the minimum AC line OVLO voltage can be determined using the minimum BULK_S OVLO threshold V_{OVLO_TH} (2.09V) and the following equation:

$$V_{AC}^{OVLO} = \frac{1}{\sqrt{2}} \cdot V_{OVLO\_TH} \cdot \left(\frac{R_{B1}}{R_{B2}} + 1\right) = \frac{2.09V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{R_{B2}} + 1\right)$$

Furthermore, the minimum AC line OVLO recovery voltage can be determined using the minimum BULK_S recovery from over-voltage threshold V_{OVLO_REC} (2.05V) and the following equation:

$$V_{AC}^{OVLO\_Rec} = \frac{1}{\sqrt{2}} \cdot V_{OVLO\_REC} \cdot \left(\frac{R_{B1}}{R_{B2}} + 1\right) = \frac{2.05V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{R_{B2}} + 1\right)$$

Design Example – Universal Line Voltage

The desired maximum brown-in voltage is set to 82Vac to ensure sufficient margin for input AC line variations and BULK_S resistor divider ratio accuracy. For this application we wish to minimize no-load power; therefore, the BULK_S pull-up resistance is chosen to be 4x22M (88MΩ). Finally, the required pull-down resistance is calculated to be equal to

$$R_{B2} = \frac{88M\Omega}{\frac{82Vac \cdot \sqrt{2}}{0.575V} - 1} = 438.5k\Omega = 438\text{K}\Omega \text{ (standard value)}$$

Utilizing R_{B1} and R_{B2} the minimum AC OVLO and AC OVLO recovery voltages are calculated

$$\text{Minimum AC OVLO : } V_{AC}^{OVLO} = \frac{2.09V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{438k\Omega} + 1\right) = 298Vac$$

$$\text{Minimum AC OVLO recovery : } V_{AC}^{OVLO\_Rec} = \frac{2.05V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{438k\Omega} + 1\right) = 293Vac$$

Step 15: VAUX_S winding voltage resistors

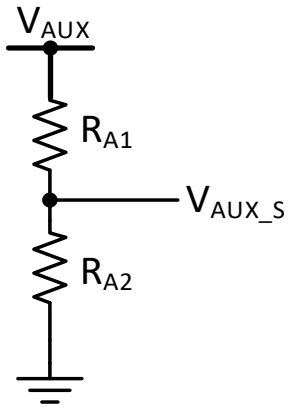

Figure 18: VAUX voltage sense circuit

VAUX_S is the sensing pin for attenuated AUX voltage and is primarily utilized to support Quasi-Resonant (QR) mode of operation. An internal QR valley comparator, connected to V_{AUX_S}, detects the QR valley points. Furthermore, QR valley comparator is used to change the mode of operation from fixed frequency DCM to valley switching DCM during start-up and to provide output short circuit protection.

For sensing the reflected voltage on the auxiliary winding, a resistor divider is placed at the V_{AUX} pin (R_{A1} and R_{A2}).

$$V_{VAUX\_S} = \frac{R_{A2}}{R_{A1} + R_{A2}} \cdot V_{AUX}$$

The optimal divider ratio depends on the maximum input and output voltage levels of the AC/DC converter, as well as the transformer turns ratios. R_{A1} and R_{A2} resistors values should be chosen such that, under no operating conditions, V_{AUX_S} pin voltage exceeds the absolute maximum voltage rating (±10V).

$$V_{AUX\_S}^{MAX} = \left(V_{OUT\_MAX} \cdot \frac{N_{AUX}}{N_{SEC}}\right) \cdot \frac{R_{A2}}{R_{A1} + R_{A2}}$$
$$V_{AUX\_S}^{MIN} = \left(V_{BULK\_MAX} \cdot \frac{N_{AUX}}{N_{PRI}}\right) \cdot \frac{R_{A2}}{R_{A1} + R_{A2}}$$

The lower resistor RA2 value should be selected considering potential pin-to-pin short condition between VAUX_S and VBULK_S. For such a fault case, it is desirable that VBULK_S be pulled down below the SZ1130 BULK UVLO, VUV_TH (258mV), for all expected input voltage operating conditions, such that SZ1130 remains in a non-switching state. Typical RA2 value required to ensure safe operation is 1/20th the value of BULK_S pull-down resistor RB2. When calculating RA1 it is recommended to add ~10% safety margin to VBULK_MAX and VOUT_MAX.

It should be noted that valley detection delays can be compensated for with the use of an external capacitor, which is placed either in parallel with R_{A2} when the valley point is early, as shown in Figure 19: , or which is placed in parallel with R_{A1} when the valley point is late, as shown in Figure 20: .

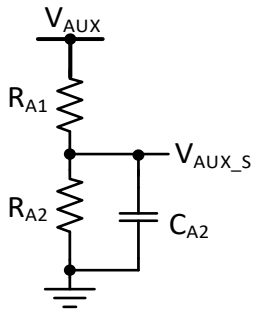

Figure 19: VAUX_S sensing circuit to add time delay.

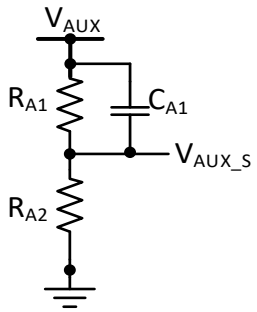

Figure 20: VAUX_S sensing circuit to add time lead.

The C_{A2} capacitor value can be calculated to meet the desired delay Δt_{delay}:

$$C_{A2} = \frac{\Delta t_{delay}}{(R_{A1} || R_{A2})}$$

The relation between feedforward capacitance C_{A1} and time lead is given below:

$$\Delta t_{lead} = \frac{T_{QR}}{360} * [\ \tan^{-1}\left(\frac{2\pi R_{A1} C_{A1}}{T_{QR}}\right) - \tan^{-1}\left(\frac{2\pi R_{A1} C_{A1}}{T_{QR}} \frac{R_{A2}}{R_{A1}+R_{A2}}\right)\ ]$$

where, T_{QR} = time period of QR resonance.

Design Example

R_{A2} value should be less than 470kΩ / 20 = 23.5kΩ, and the closest E24 value is 22k.

The R_{A1} value can be calculated as

$$V_{AUX\_S}^{MAX} = \left(V_{OUT\_MAX} \cdot \frac{N_{AUX}}{N_{SEC}}\right) \cdot \frac{R_{A2}}{R_{A1}+R_{A2}}$$

$$10 = \left(20\text{V} * 1.1 * \frac{14T}{5\text{T}}\right) \cdot \frac{22\text{k}}{R_{A1}+22\text{k}}$$

R_{A1} = 113.52k

$$V_{AUX\_S}^{MIN} = \left(V_{BULK\_MAX} \cdot \frac{N_{AUX}}{N_{PRI}}\right) * \frac{R_{A2}}{R_{A1}+R_{A2}}$$

$$-10 = \left((-265\text{Vac} * 1.414 * 1.1) * \frac{14T}{36\text{T}}\right) * \frac{22\text{k}}{R_{A1}+22\text{k}}$$

R_{A1} = 330.66k

To satisfy both polarities of maximum voltage rating, RA1 = 330kΩ is selected for the design.

For a delay Δt = 100ns, the capacitor is calculated as

$C_{A2} = \frac{100\text{ns}}{(330k||22\text{k})}$ = 4.85pF = 5.1pF (Standard value)

Step16: OTP sensing

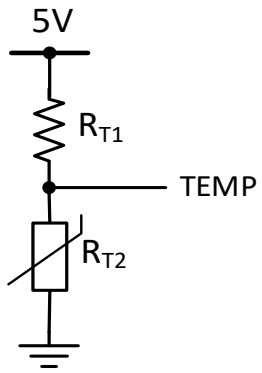

Figure 21: **Over temperature sensing circuit**

A second temperature monitor is provided by an external NTC (negative temperature coefficient) thermistor. The R_{T2} connected from TEMP pin to ground can be used to give over-temperature protection to the power supply from hotspots on the printed circuit board. At start-up, the voltage at TEMP needs to be higher than V_{NTCR} =1V for the IC to start operation. If the voltage at TEMP is lower than V_{NTCTH} = 0.61 after the start-up, the IC shuts down and recovery from shutdown takes place once the voltage is above 1V.

Once OTP set point and R_{T2} are determined the pull-up resistor R_{T1} can be determined using the minimum TEMP_S threshold V_{NTC_TH} (0.61V) and the following equation:

$$\text{V\_NTCTH} = 5 \cdot \frac{RT2@120\mathring{0}C}{RT1 + RT2@120\mathring{0}C}$$

Design Example

NCP15WL104E03RC (100k resistor at 25°C)is selected as the NTC resistor for the reference design. For a desired external OTP set point of 95degC. RT1 pull up resistor is calculated as:

$$\text{V\_NTCTH} = 5 \cdot \frac{RT2@95^{o}C}{RT1 + RT2@95^{o}\,C}$$

$$0.61V = 5V \cdot \frac{5.7\text{k}}{\text{RT1} + 5.7\text{k}}$$

RT1 = 41k

Step 17: OOVP_S sensing resistors

The OOVP_S pin senses the reflected output voltage through the auxiliary winding using a resistor divider circuit connected after the auxiliary rectifying diode as shown in Figure 22. During start-up, output over-voltage protection is triggered when the voltage at pin OOVP_S exceeds V_{OOVP_TH} (1.4V). Recovery from output over-voltage condition requires OOVP_S pin voltage to drop below V_{OOVP_REC} (1.08V). During steady state, output over-voltage protection is provided by sensing the VFB pin voltage, specifically when FB is pulled up to V5OUT for extended period of time.

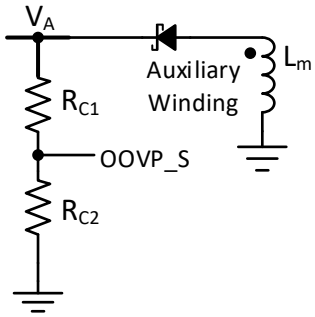

Figure 22: Resistor Divider for Output OVP Sensing

The following equation calculates the voltage at OOVP_S pin.

$$V_{OOVP\_S} = \frac{R_{C2}}{R_{C1} + R_{C2}} . V_A$$

Where, V_A is the rectified auxiliary voltage, as shown in Figure 22.

The lower resistor R_{C2} value, like R_{A2}, should be selected considering potential pin-to-pin short condition between V_{OOVP_S} and V_{BULK_S}. For such a fault case, it is desirable that V_{BULK_S} be pulled down below the SZ1130 BULK UVLO, V_{UV_TH} (258mV), for all expected input voltage operating conditions, such that SZ1130 remains in a non-switching state.

Note: It is also recommended to use a Zener diode (connected between the Anode of the optocoupler and SGND) to provide Output over voltage protection in case of USB -PD IC VFB to SGND single-point failure.

Maximum Output Voltage	OOVP Zener	OOVP Voltage
5	MMSZ5235B	9
9	MMSZ5241B	14
12	MMSZ5245B	18
15	MMSZ5248B	21
20	MMSZ5251B	25
21	MMSZ5251B	25
24	MMSZ5252B	27

Table 5: Recommended Output Over Voltage protection Zener with respect to the Maximum output voltage.

Design Example

R_{C2} is selected to be equal to R_{A2}, 22k. With the output OOVP threshold set to 8V, the corresponding reflected voltage on auxiliary winding, V_A is calculated as:

$$V_A = V_{OUT} \cdot \frac{Naux}{Nsec} = 8V \cdot \frac{14T}{5T} = 22.4V$$

R_{C1} can now be calculated using the equation,

$$V_{OOVPS} = \frac{R_{C2}}{R_{C1} + R_{C2}} . V_A$$

$$1.4 = \frac{22k}{R_{C1} + 22k} \cdot 22.4\text{V}$$

R_{C1} = 330kΩ

Step 18: Conducted EMI Filter design

The Conducted EMI noises are generated from power supplies due to the switching actions of the semiconductor devices. Although the EMI regulation specifications (CISPR22-Class B) target the total EMI emission for SMPS, the noises can be categorized into differential-mode and common-mode noises in order to minimize each noise more effectively for an overall emission suppression.

In low frequency band (< 400kHz), differential mode noise is usually the main noise source, and the common mode noise is dominant at high frequency range. Due to circuit parasitic and fast switching nature of power devices, extra effort is required to determine the noise attenuation requirement at the ultra HF band, typically in the frequency range of 5M to 20MHz. Since the circuit parasitic is difficult to quantize, the EMI design is usually an iterative effort following steps as described below.

1. Determine the attenuation requirement on the differential mode noise.
   The nominal switching frequency of the converter is ~100kHz and since the CISPR-22 starts with 150kHz. The harmonics of interest would be the 1st to 3rd harmonics of switching frequency noise in the range of 200kHz to 300kHz.

2. Determine the attenuation requirement on the common mode noise.
   The Quasi Resonance frequency generates main CM noise in the 600kHz range. The good approach is to determine the CM inductance requirement at this frequency band.

3. To attenuate the ultra HF noise, usually from the circuit parasitic and switching power devices, an additional small CMC, with minimum parasitic capacitance is required.

In addition to the common mode & differential mode chokes, X- cap (connected between Line and Neutral) and Y-cap (connected between primary and secondary ground) are used to filter out the noises. The Y capacitor provides a low impedance return path for currents generated by the switching voltages between the primary and secondary windings of the transformer. A well-designed Transformer with noise cancelling technique would require a smaller Y cap.

Recommended values

CMC Choke 1 = 8mH

CMC Choke 2 = 350uH

X-cap =100nF (X-cap should be no higher than 200nF).

Y-cap = 330pF

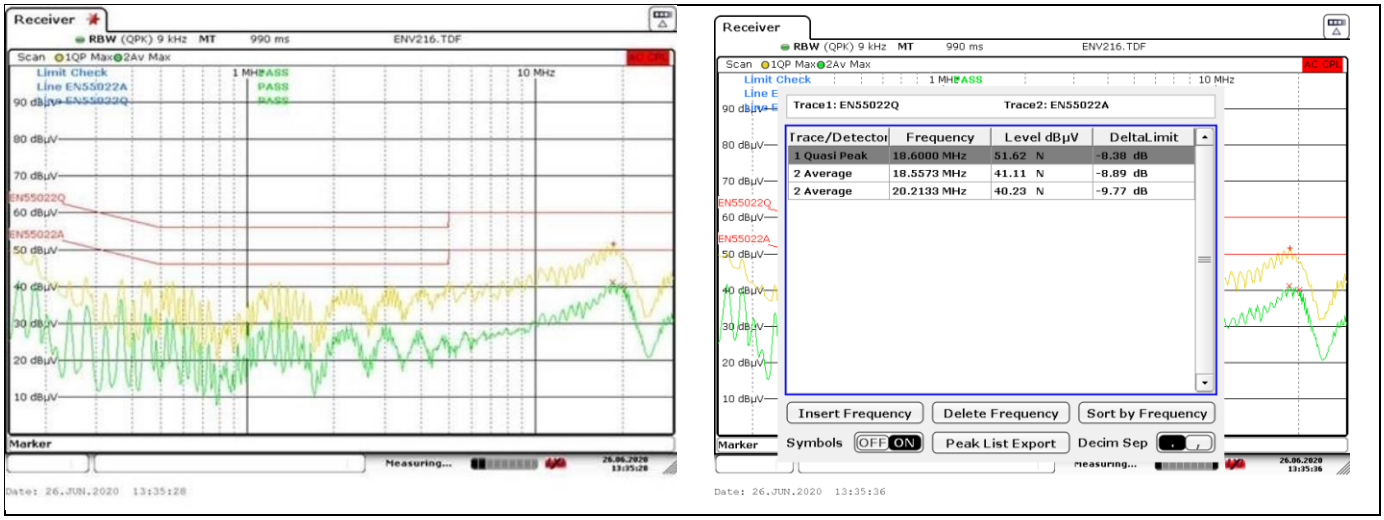

Figure 23: Conducted EMI spectrum captured on our EVB with grounded output at high line (230Vac) and 5V output , 3.25A load.

Step 19: Compensation circuit

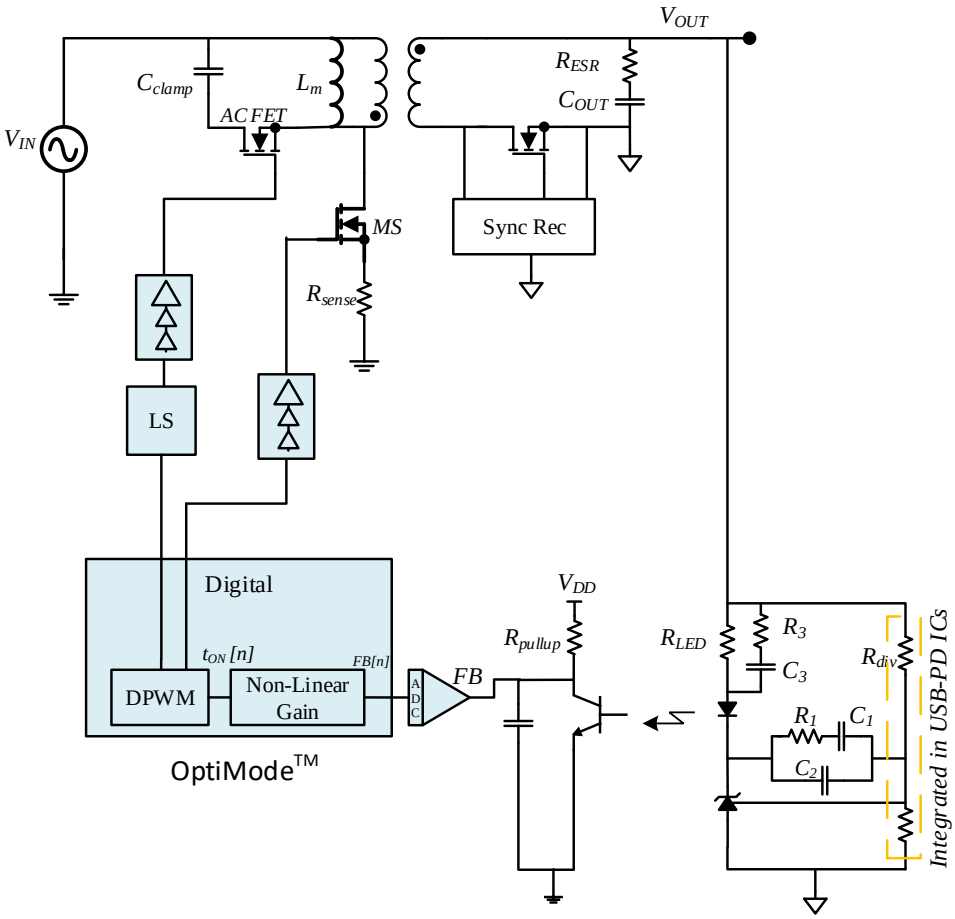

Figure 24: Compensation Circuit

The SZ1130 device uses pin 12 (FB) to regulate the secondary side output voltage. FB is connected to the open-collector output of an opto-isolator and an external feedback resistor, R_{pullup} to pin 13 (V5OUT). The open collector transistor sinks current from pin 13 (V5OUT) and modulates the FB voltage level depending on the output voltage error. The FB voltage is utilized by SZ1130 to determine the required pulse width of the primary side FET and in such a way achieve tight output voltage regulation.
In order to design a suitable compensator for SZ1130, best control theory practices should be used in order to ensure enough phase and gain margin are achieved for all operating conditions.

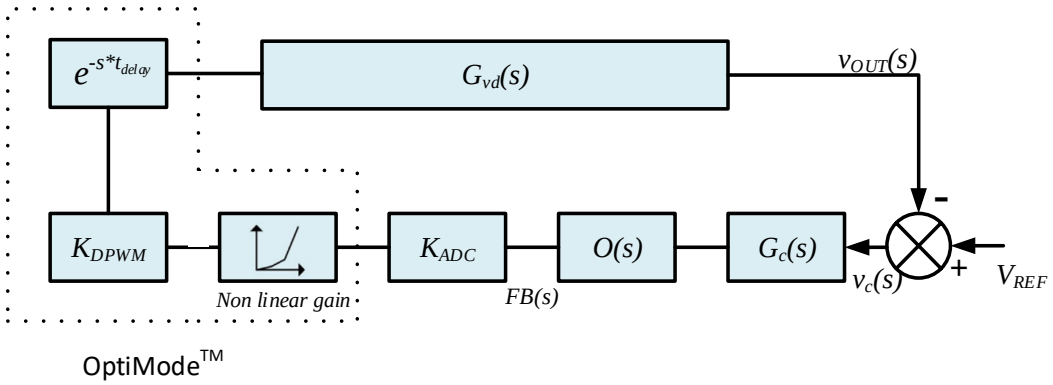

Figure 25: OptiMode gain block diagram

Control to output transfer function

Control to output transfer function of the flyback converter operating in QR mode of operation, $G_{vd}(s)$ is determined with the following equations:

$$G_{vd}(s) = \frac{v_{OUT}(s)}{d(s)} = G_{vd0} \cdot \frac{\left(1 + \frac{s}{w_{dz}}\right) \cdot \left(1 - \frac{s}{w_{rhz}}\right)}{\left(1 + \frac{s}{w_{dp}}\right) \cdot \left(1 + \frac{s}{w_{hfp}}\right)}$$

where, dc gain, G_{vd0} and dominant zero and pole, w_{dz} and w_{dp} are given with:

$$G_{vd0} = \frac{V_{OUT}}{D} = \frac{V_{IN}^2 \cdot t_{ON}}{2L_{m.pri} \cdot I_{OUT}}$$

$$w_{dz} = \frac{1}{C_{OUT} \cdot R_{ESR}}$$

$$w_{dp} = \frac{2}{C_{OUT} \cdot V_{OUT}/I_{OUT}}$$

where C_{OUT} is the effective capacitance at the output, $L_{m,pri}$ magnetizing inductance reflected on the primary, R_{ESR} equivalent series capacitance of the output capacitor, V_{IN}, V_{OUT} and I_{OUT} operating conditions.

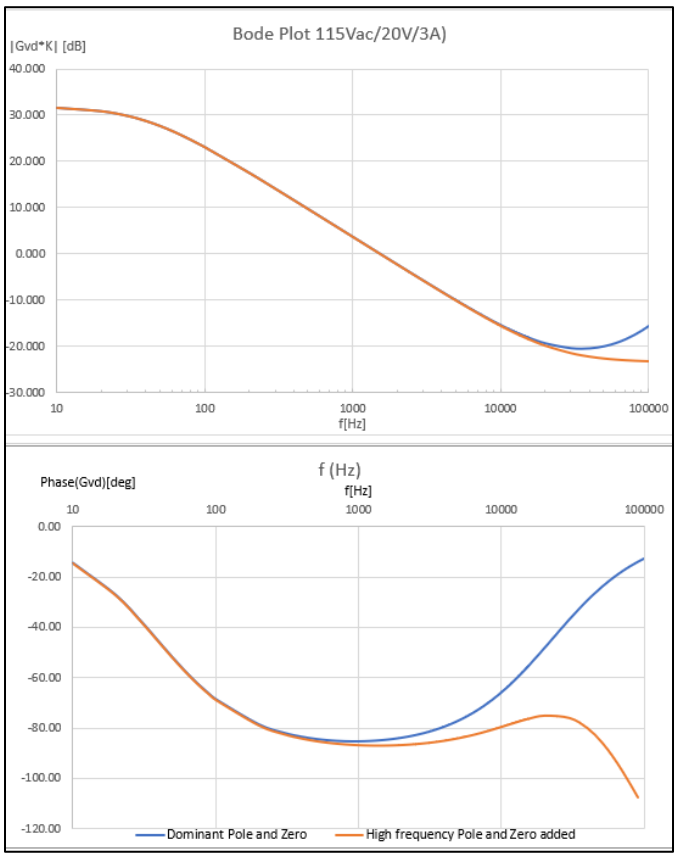

Figure 26: Bode Plot of G_vd (s) of 65 W reference design for 115AC/20V/3.25A operating point.

High-frequency pole and right half plane zero, w_{hfp} and w_{rhz}, are not salient features of the control-to-output transfer function for converters operating in discontinuous conduction mode nevertheless their effect can be taken into the account using following equations:

$$w_{rhz} = \frac{2f_S}{D}$$

$$w_{hfp} = \frac{2Mf_s}{D}$$

where f_S is the switching frequency, $D = t_{ON}f_S$ duty ratio and $M = \frac{V_{OUT}n_S}{V_{IN}n_p}$ normalized conversion ratio of the converter. To demonstrate the effect of the high frequency pole and right half plane zero, bode plot of the control to output transfer function, $G_{vd}(s)$, of the 65 W reference design for 20V/3.25A/115ac operating point is plotted in Figure 26. As shown in Figure 26 phase drop due to non-dominant features can be up to 10° at frequencies around 10 kHz.

SZ1130 transfer characteristics

As show in Figure 25: and Figure 26: blocks that are part of SZ1130 and affect the total loop gain of the system are pulse-width modulator (PWM), non-linear gain modulator and the internal Analog to Digital Convertor (ADC). The gains of the PWM block and the ADC block inside the SZ1130 are given with: $K_{DPWM} = f_S/42e3$ and $K_{ADC} = 2^8/5$.

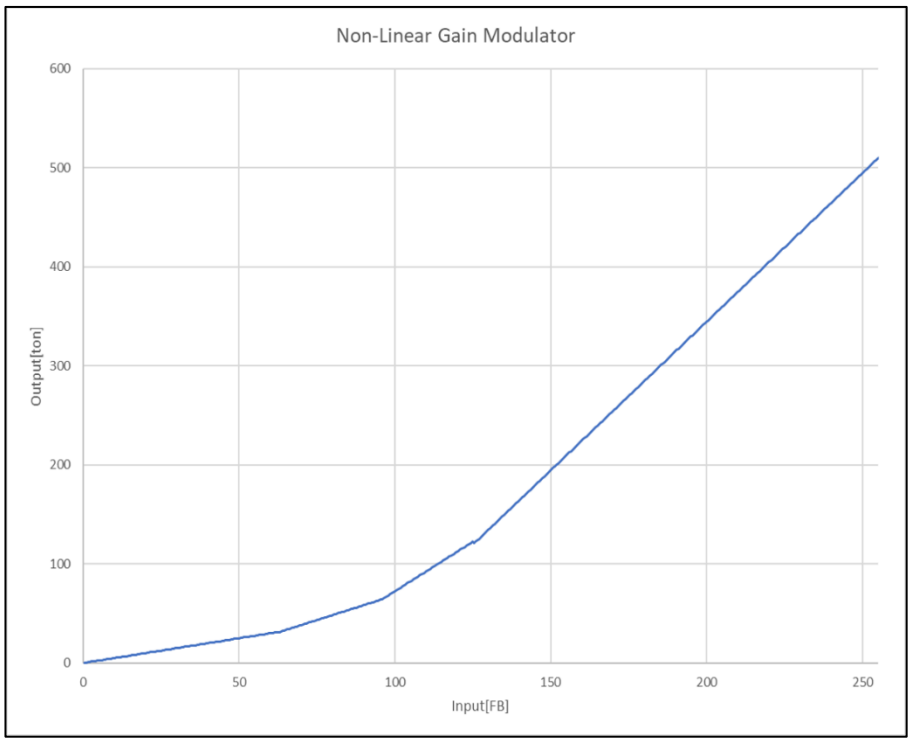

Figure 27: Non-linear transfer function

The non-linear gain modulator is Silanna's proprietary functional block which modulates the digital value of the feed-back (FB) signal to achieve the constant loop gain across different line voltages. The other form of equation for the dc gain of the converter G_{vd0} contains $V_{IN}^2 \cdot t_{ON}$ product, thus, to equalize this product across different line voltages, FB signal which represents the t_{ON} is being modulated with $\sim x^2$ function as shown in Figure 27.

Delay that affects the phase characteristics is given with: $t_{delay} = t_{ON} + T_S$ where t_{ON} represents the delay through PWM modulator and T_S is the switching frequency and represents the conversion time from the input of the ADC to the PWM blocks.

Design Example – Gain Determination through the SZ1130

For a FB value of 3V, switching frequency = 120 kHz.

Value of the signal at the output of the internal ADC FB[n] = $(\text{FB\_value} * K_{ADC}) = \frac{3 * 2^8}{5} = 153$

Value of the signal at the output of the Non-Linear Gain Modulator FB[n] = 307 → ton[n] = 203 [From graph]

Value of the signal at the output of the DPWM block = $\frac{203 * 120 * 10^3}{42 * 10^6} = 0.58 < 1$

Gain between FB(s) and d(s) = $\frac{307 * 2^8 * 120 * 10^3}{203 * 5 * 42 * 10^6} = 0.22$

Type III Compensator Design

$$G_C(s) \cdot O(s) = \frac{V_{FB}(s)}{V_C(s)}$$

$$G_C(s) \cdot O(s) = \frac{\left(1 + \frac{s}{w_{z1}}\right) \cdot \left(1 + \frac{s}{w_{Z2}}\right)}{\frac{s}{w_I} \cdot \left(1 + \frac{s}{w_{p1}}\right) \cdot \left(1 + \frac{s}{w_{p2}}\right)} \cdot CTR \cdot \frac{R_{PUllup}}{R_{LED}} \cdot \frac{1}{1 + \frac{s}{w_{OC}}}$$

Where dominant poles and zeros are given with the following equations:

$$w_I = \frac{1}{R_{DIV} \cdot (C_1 + C_2)}$$

$$w_{P1} = \frac{1}{R_3 \cdot C_3},$$

$$w_{z1} = \frac{1}{(R_{DIV} + R_1)(C_1 + C_2)}$$

$$w_{z1} = \frac{1}{(R_3 + R_{LED})C_3}$$

CTR is current transfer ratio of the optocoupler and w_{OC} is the dominant pole of the optocoupler. CTR is dependent on temperature, current flowing through the photo diode and its value can vary up to three times depending on the operating condition. It is recommended that during the compensator design highest value of the CTR from datasheet is assumed since that will yield worst phase margin.

Dominant pole of the optocoupler, w_{OC} also depends on the bias current of the optocoupler and usually is not given explicitly in the datasheet. Thus, it is recommended that it should be experimentally tested in the laboratory before designing the compensator. Optocoupler, TLP383, used in 65W reference design is characterized experimentally

using the circuit shown in Figure 28 and w_{OC} is plotted in terms of the different bias currents of the optocoupler in Figure 29. For the compensator design worst case, i.e. lowest dominant pole should be selected.

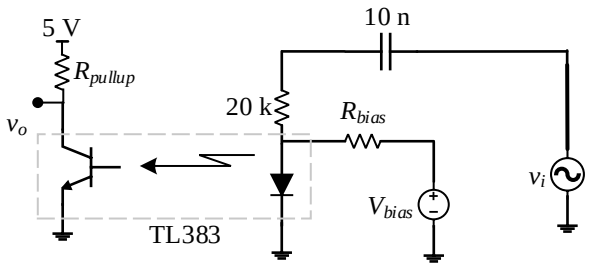

Figure 28: Circuit for optocoupler characterization

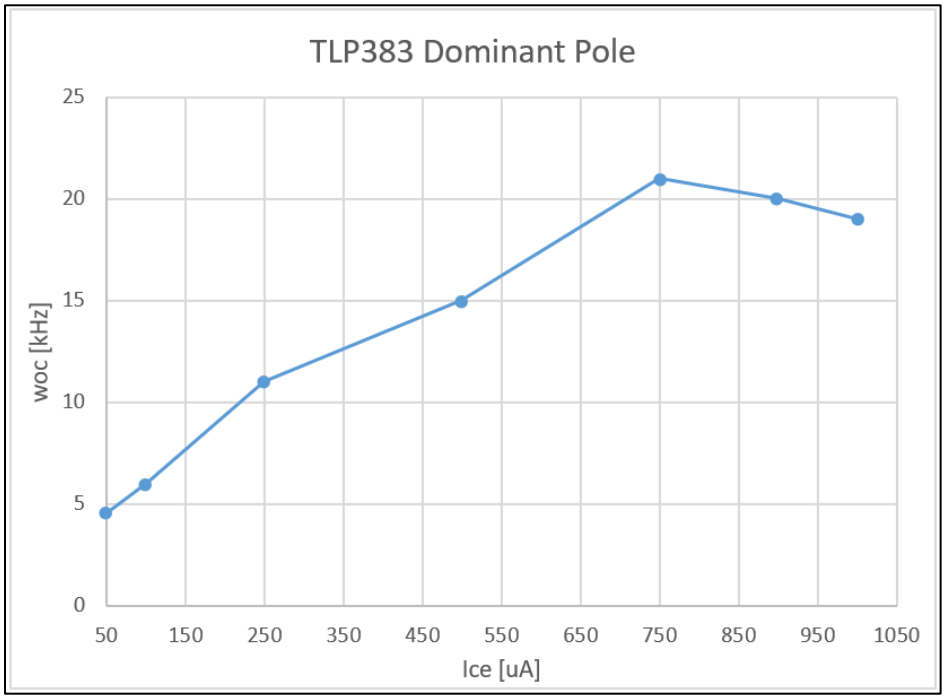

Figure 29: TLP383 optocoupler dominant pole for different bias currents.

Design Example –Compensator SZ1130

To ensure stability of the system phase margin should be selected to be higher than 45deg across all operating conditions. The worst-case scenario (minimum phase margin) occurs at 5V/3A and high line.

The system parameters:

Vout	5.00	V
Vac	295	V
fs	9.06E+04	Hz
Lm(primary)	2.90E-04	H
Cout	1.33E-03	F
Resr (DataSheetNom)	7.00E-03	Ohm
Iout	3	A
N	7.2	
eff	0.92	

Calculated variables of the Gvd(s) using provided tool:

M	0.0865	
R	1.666666667	Ohm
ton	6.99E-07	s
D	6.59E-02	
fs	9.42E+04	Hz
wz (dominant zero)	1.51233081E+05	rad/s
wp (dominant pole)	9.12999821E+02	rad/s
Gvd0 (dc gain)	7.59E+01	V
wp2 (high f pole)	2.49E+05	rad/s
wrhp (right half plane zero)	2.86E+06	rad/s
cycle delay	1	

In order to compensate the effect of the dominant pole of the plant and dominant pole of the optocoupler two zeros of type III compensator are placed such that in a range of 1Khz to 10Khz phase boost of up to 60deg is achieved.

Controller Parameters TYPE III		
Rdiv	7.50E+05	Ohm
R1	4.70E+03	Ohm
C1	3.30E-08	F
C2	3.30E-08	F
Rpullup	8.20E+03	Ohm
Rled	6.20E+03	Ohm
Ct_total	4.70E-10	F
R3	1.50E+03	Ohm
C3	8.20E-09	Ohm

wz_c1 (dom)	202.0202	rad/s
wp_c1	12894.9065	rad/s
wi_c (dom)	202.0202	rad/s
wz_c3 (dom)	15837.8207	rad/s
w_p1	81300.81301	rad/s
w_oc(measured)	31400.0000	rad/s

Outputs:		
Phase Margin:	93.15	deg
at frequency	5400	[Hz]
Index:	63.00	
Gain Margin	11.2608753	dB
at frequency	20000.00	[Hz]
Index gain	167	

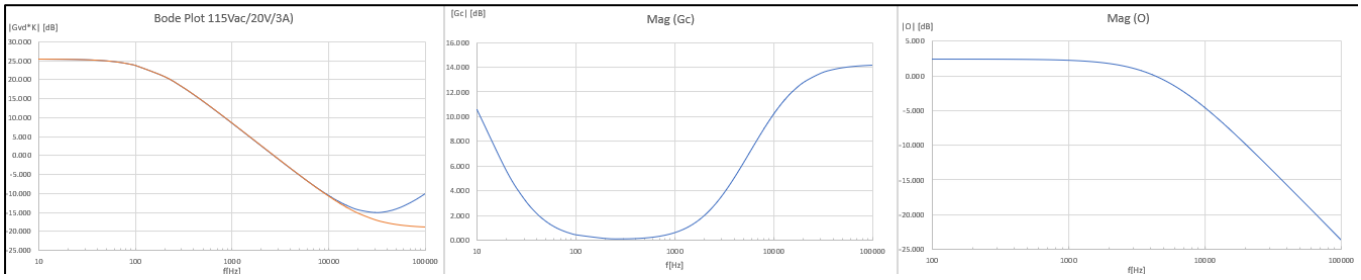

Figure 31: Plant transfer function, $\boldsymbol{G_{vd}(s)}$, controller transfer function $\boldsymbol{G_c(s)}$ and optocoupler transfer function $O(s)$.

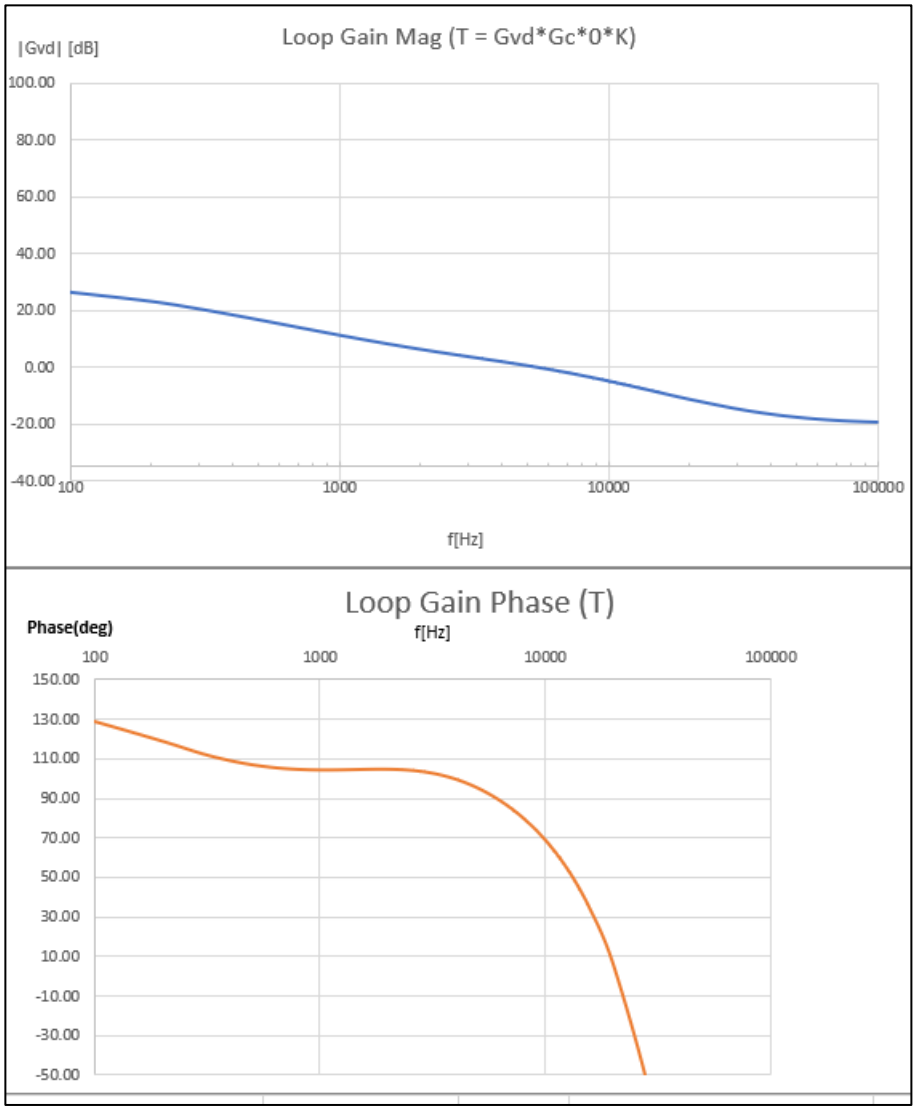

Figure 32: Loop Gain,$T_S(s) = G_{vd}(s) \cdot G_c(s) \cdot O(s) \cdot K$ for the 5V/3A/295ac operating condition of the 65W reference design.

Revision History

Date	Revision	Notes	Author
08/06/2020	1.0	Initial Release	Rakshitha Salian