JOB DESCRIPTION – POWER IC DESIGN ENGINEER

POSITION SUMMARY:

The IC Design Engineer will be responsible for designing analog and mixed signal blocks for integrated POL, Multiphase and PMIC power management products. Mentors will be available to guide and advise as needed, but some level of autonomy is expected with respect to design, investigation, simulation and professional development. There will also be some limited level of interaction with cross-functional teams such as Applications & Test Engineering.

REPORTS TO: Manager or Director of Design Engineering

LOCATION: TBD

QUALIFICATIONS:

Education: BSEE Required; MSEE preferred.

Experience: Any professional experience in analog and mixed signal IC design of power management circuits is a plus. 1-5 years preferred.

Core Competencies:

Strong knowledge of analog integrated circuit fundamentals
Strong knowledge of CMOS device physics and fabrication processes
Knowledge of parasitic and noise analysis
Knowledge of best Layout practices
Self-motivated, driven, and passionate individual with focus on results and meeting project schedules
VerilogA or AVHDL language and simulation verification experience is a plus
Mixed-signal simulation, interfacing with analog functions - Fluent with Cadence design environment
Must possess strong written and verbal communication skills

ESSENTIAL DUTIES & RESPONSIBLITIES:

1. Participate in several aspects of the design cycle, including transistor level design, layout supervision, lab debug of your cells
2. Research and development of state-of-the-art analog and mixed signal products for selected markets
3. Work with other members of Design to develop Power Management Cell IP including but not limited to Buck Regulators, Boost Regulators, LDO, Bandgap, Voltage and Current References, Clock, bias circuitry, etc.
4. Develop products to meet the performance and cost targets on time
5. Preparation of cell IP support documents. Present cell IP to peers
6. Provide guidelines to Mask designers on circuit layout
7. Author characterization and cell test plans for the IPs and Product
8. Travel will be rare. Less than once per year typically