DC/DC Buck Converter Input Bypassing Layout Guide

DC/DC buck converter

The simple and ubiquitous DC/DC buck converter has improved markedly in recent years. One notable area of improvement is the speed at which the switching transition takes place. This increase in speed however presents special challenges to bypassing the input supply V_{IN}. The turn on event of the high side switch in a synchronous converter produces a high di/dt that, if not properly bypassed, can result in large dips on the input supply that can disturb other circuitry on that same power rail. The event can also produce excessively large ring amplitudes visible at the switched node of the converter.

Silanna *ZqFET™* technology is extremely fast switching, rivaling GaN devices, and special attention to the design of the input supply bypass should be given. This application note describes the importance of and guidance towards applying good layout techniques to achieve adequate bypassing of the input supply.

Consider the equivalent circuit of a buck converter in Figure 1. The relevant parasitic components of the power devices are shown, and the output filter has been replaced with a current source. No other parasitics are shown at this time.

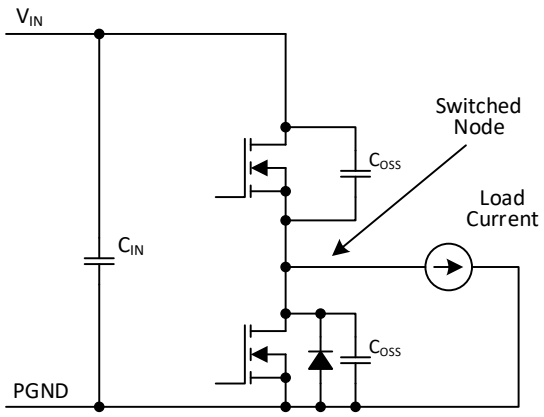

Figure 1. Typical Application Diagram

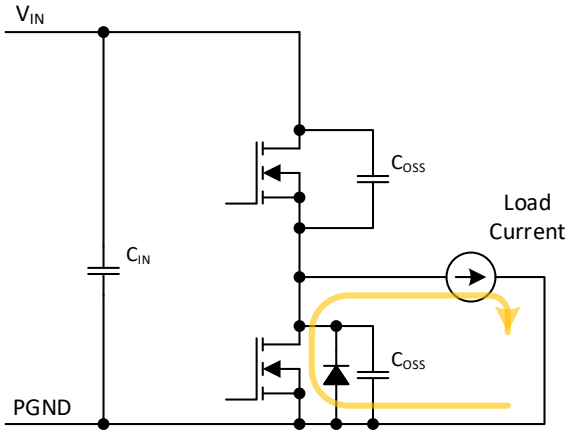

Figure 2: Current loop before high side device turn on

Preceding the turn on of the high side device, the channel of the low side device is in the off state and the load current flows in a loop through the parasitic body diode of the low side device as shown in Figure 2.

Current loop

As the high side device turns on, there is a new current loop introduced as shown in Figure 3. The loop looks like short circuit to GND – and it is for a brief time. During this time, the current in this loop must instantaneously provide the reverse recovery charge for the low side parasitic body diode and build to a level that equals the load current. Hereafter, the parasitic C_{OSS} capacitor of both FETs must charge from GND to V_{IN} as the switched node rises to the input voltage. This presents a low impedance path that can build current to relatively high levels very quickly.

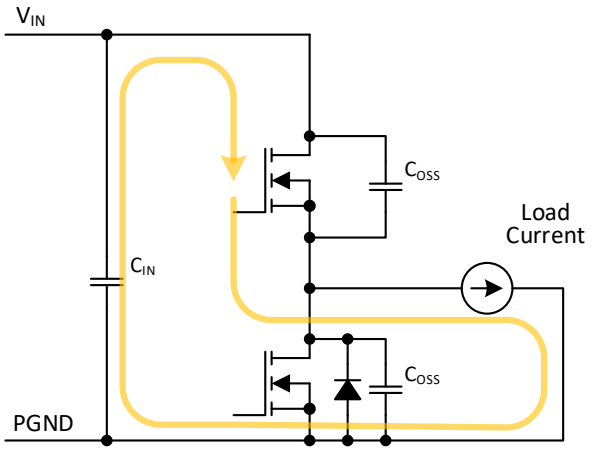

Figure 3: Current flow at time of high side device turn on

Parasitic components

The other parasitic components of concern in the system are the primary inductive components that exist in the input loop as shown in Figure 4. They include the internal package inductance of the power devices shown as L_{PKG} (lumped here into a single element), the equivalent series inductance (ESL) of the input bypass capacitor as L_{ESL}, and the inductance introduced by the layout routing of the input bypass capacitor as L_{LAYOUT}.

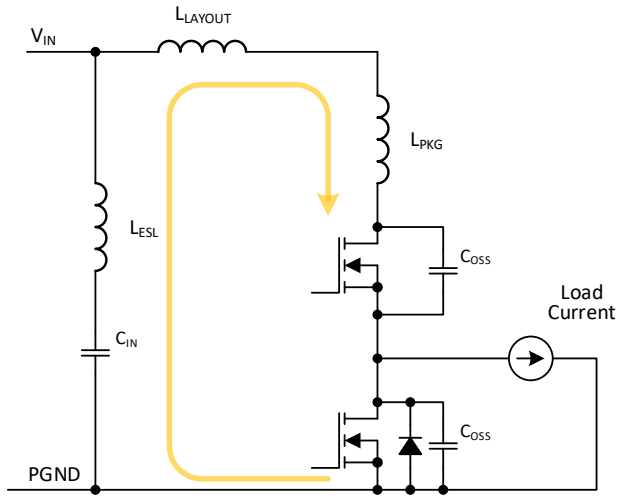

Figure 4: Inductive parasitic components in the input loop

Of these, the largest and most influential is L_{LAYOUT}. Fortunately, it is also the component which the power supply designer has the most control over. These parasitic inductances limit the rise time of the current when the high side device turns on, forming a resonant circuit with the C_{OSS} parasitic capacitor of the low side FET. The high side C_{OSS} is shunted out of the resonant circuit because the high side channel is turned on. Minimizing the size of L_{LAYOUT} can pay big dividends in reducing ring and voltage stress on the power devices.

Layout

What influences the size of L_{LAYOUT}? The primary consideration is the size of the current loop – its physical area. Therefore, the goal to optimizing the layout of the input bypass capacitance should be to minimize the current loop area in Figure 4.

Typically, there will be multiple capacitors comprising C_{IN} used to bypass the input voltage. These capacitors should have a small value capacitor in a small footprint located as close as possible to the power switches to provide a low impedance to high frequency currents. For the purposes of ringing and EMC, this small capacitor is essentially all that matters. The layout of the rest of the bulk input capacitance should minimize, to the extent possible, the inductive loop it presents, but it is secondary to this first small capacitor next to the power switches.

Consider a layout as shown in Figure 5. This is a single layer V_{IN} layout using the Silanna F44 QFN package.

Note: The V_{IN} copper pour area in this figure does not have a soldermask opening for pin 12. See the datasheet for recommendation on the footprint.

The red path is the rough current path taken by the loop highlighted in Figure 4.

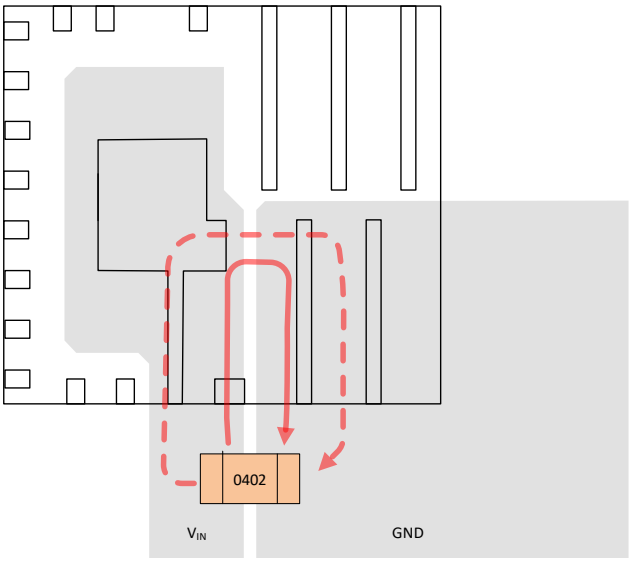

Figure 5: Single layer current loop

One should note that the actual current path is frequency dependent with higher frequency components tending to travel closer to the inner boundaries of the copper pours and lower frequency components in more direct straight-line routes.

The scope of this document emphasizes the frequencies important to switch node ringing and EMC compatibility. Therefore, the high frequency current path is primarily of importance in the input decoupling.

Figure 5 is the optimal layout for a single layer implementation. Note that the capacitor is placed as close as possible to the power device pins. In this case, the drawing is to scale, and the component separation is 0.5 mm, a common design rule minimum.

Most DC/DC converters operate in environments where multiple layer boards are the norm. A typical 4 layer board stackup is shown in Figure 6. Having multiple layers presents the possibility of creating lower inductance loops and requires thinking in three dimensions instead of two.

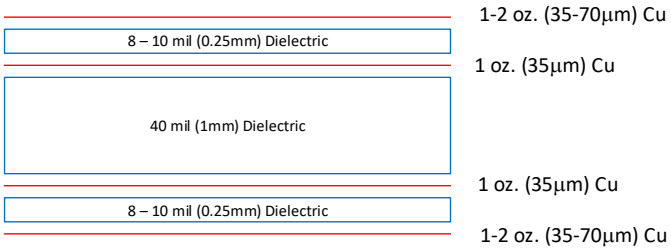

Figure 6: Typical 4 layer board stackup

Consider the layout in Figure 7. The previous layout from Figure 5 has been placed over a GND plane on layer 2. High frequency currents can now find a lower inductance path through the power switches to the V_{IN} bypass capacitance.

Note: The top layer V_{IN} copper pour area in this figure does not have a soldermask opening for pin 12. See the datasheet for recommendation on the footprint.

The GND current can travel to the GND plane where it is freer to truly mirror the V_{IN} current path in the V_{IN} pour on the top layer, rather than being confined to the copper pour on the single layer (the top layer).

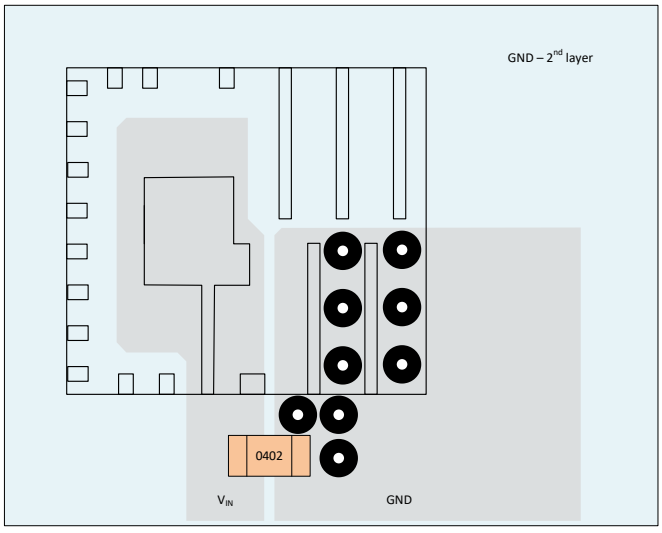

Figure 7: V_{IN} over ground plane

Another potential option for decoupling the input loop is to place the decoupling components on the bottom side of the PCB, directly underneath the power switches. Figure 8 shows the typical ring waveform with V_{IN} bypass caps located 0.5 mm from the power switch package on the top layer along with an additional capacitor placed directly beneath the V_{IN} and GND pads on the bottom layer.

Figure 9 shows a zoomed in view of the waveform of Figure 8 (white trace in Figure 9) with the bottom-side capacitor present overlaid with the waveform obtained when the bottom side capacitor is removed (green trace in Figure 9). Note that there is very little difference in the ring waveform. The frequency without the bottom side capacitor is slightly lower and the amplitude is slightly higher than with the bottom-side capacitor. Both observations point to a slightly increased effective inductance without the bottom side capacitor.

Therefore, excluding the bottom-side capacitor is usually fine for the performance of the design.

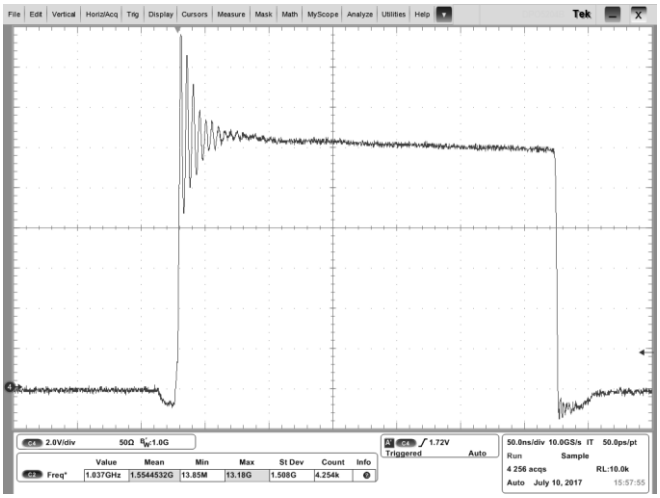

Figure 8: Typical ring waveform with F44 package

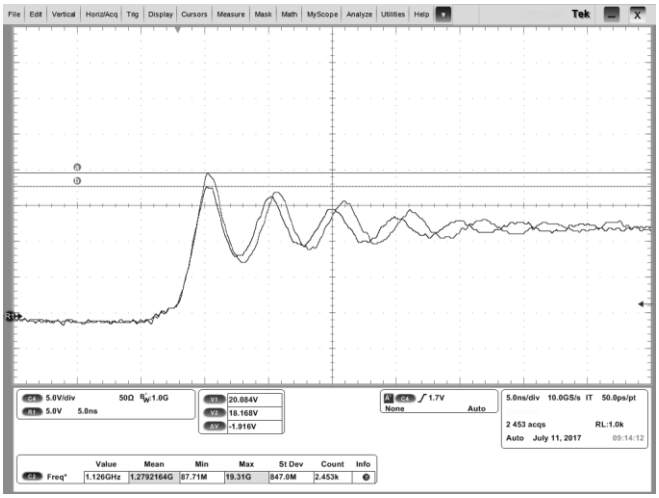

Figure 9: Comparison of with/without bottom-side capacitor

Revision History

Date	Revision	Notes	Author
February 28, 2018	1.0	Initial Release.	KH
April 30, 2018	2.0	Reformatting and text edits.	AR
July 15, 2019	3.0	Text edits. Update headers/footers and update to new logo.	CR