## Flyback PWM Controller with Integrated Active Clamp Circuit

#### **Features**

- Integrated UHV Active Clamp FET, Active Clamp Driver, and Start-up Regulator
- Capable of Over 93% Efficiency
- Flat Efficiency Across Universal (90 265 Vac) Input Voltage and Load
- Tight Switching Frequency Regulation for Improved Input EMI Filter Utilization
- Up to 146 kHz Switching Frequency Operation
- OptiMode™ Cycle-by-Cycle Adaptive Digital Control
- Multi-Mode Operation (Burst Mode, QR, VMS)
- QR Valley Mode Switching for low EMI
- Self-Tuning Valley Detection
- OTP, OVP, OCP, OOPP and OSCP Protections
- <50 mW No Load Power Consumption</p>
- Up to 33 W Output Power
- 16-pin SOIC Package

### **Applications**

- High Power Density AC/DC Power Supplies
- High Efficiency Power Adapters
- USB-PD/QC AC/DC Power Adapters
- · Battery Chargers for Mobile Devices

#### **Application Diagram**

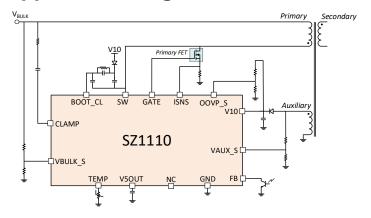


Figure 1: Active Clamp Flyback Controller

#### **Product Description**

The SZ1110 is an Active Clamp Flyback (ACF) PWM Controller that integrates an adaptive digital PWM controller and the following Ultra High-Voltage (UHV) components: active clamp FET, active clamp driver and a start-up regulator.

The device provides ease-of-design of a simple flyback controller with all the benefits of an ACF design, including recycling of the leakage inductance energy of the flyback transformer and limiting the primary FET drain voltage spike during the turn-off events. Employing Silanna's OptiMode<sup>TM</sup> digital control architecture, the SZ1110 adjusts the device's mode of operation on a cycle-by-cycle basis to maintain high efficiency, low EMI, fast dynamic load regulation and other key power supply parameters in response to varying line voltage and load.

Furthermore, the switching frequency is confined within a tight frequency band for simplified EMI filtering. In addition, adaptive digital control of active clamp operation enables near ZVS turn-on of the primary FET and clamps the drain voltage during the turn-off, thus further improving efficiency and reducing EMI.

Unlike conventional ACF designs, tight tolerances of the clamp capacitor and leakage inductance values are not required for proper operation of the circuit in high volume production. Moreover, a small 3.3 nF clamp capacitor is sufficient to realize the benefits of ACF operation. The SZ1110 is well suited for high efficiency and high-power density AC/DC power adapters. The device is designed for up to 33 W output power, including USB-PD and Quick Charge applications.

The SZ1110 is available in a space saving 16-pin SOIC package.

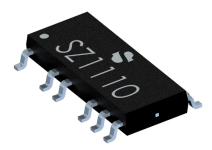


Figure 2: Device Package Image



PRODUCT BRIEF SZ1110

### **Pin Out**

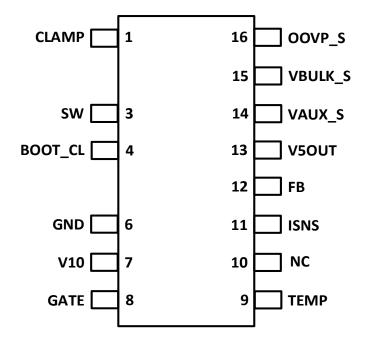


Figure 3: SZ1110, SOIC16, 1.27 mm Pitch Package Pinout – Device Top View

#### **Pin Definitions**

Pin #	Name	Voltage Category (Vdc)	Description
1	CLAMP	UHV (620V)	Drain of Active Clamp (ACL) FET. Connect through a clamp capacitor to VBULK
3	SW	UHV (620V)	Switching node. Connect to transformer primary and Drain of the Primary N-FET
4	BOOT_CL	UHV (620V)	Bootstrap supply input for internal ACL FET driver. Connect bootstrap capacitor charging circuit from V10 Pin. See BOOT_CL Pin description
6	GND	LV (0)	Power ground pin for the IC. Connect to GND
7	V10	LV (10V)	Supply voltage input, 9.5 V nominal
8	GATE	LV (10V)	Gate driver output for Primary N-FET (refer to V10)
9	TEMP	LV (5V)	External NTC temperature sensor input
10	NC	Floating Pin	No Connect. Keep this pin floating. Do not connect to any nets
11	ISNS	LV (5V)	Current sense input. Connect to the positive terminal of the current shunt resistor
12	FB	LV (5V)	Output voltage error input (feedback). Connect to the Optocoupler collector and pull up to V5OUT
13	V5OUT	LV (5V)	Output and decoupling pin for the internal +5 V supply
14	VAUX_S	LV: (8V)	Auxiliary winding sense input for QR operation. Connect the auxiliary positive terminal to this pin via a resistor divider
15	VBULK_S	LV: (5V)	VBULK sense input. Connect to the rectified input voltage (VBULK) via a resistor divider
16	OOVP_S	LV: (5V)	Output over-voltage sense input. Connect to auxiliary winding (after Schottky diode) via a resistive divider

PRODUCT BRIEF SZ1110

# **Typical Application Circuit**

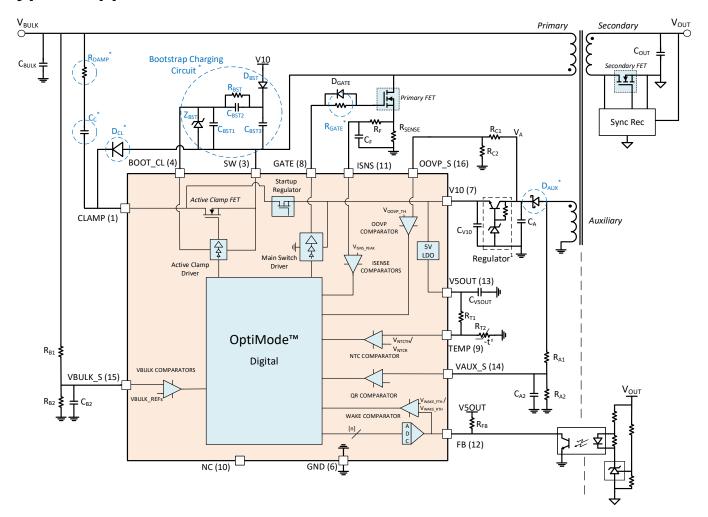


Figure 4: Typical Application Circuit of an Active Clamp Flyback Converter using SZ1110

#### Notes:

- \* Critical components are identified with **blue** dotted circles. Careful considerations are required when selecting these components for reliable operation of the device.
- 1. The discrete regulator is required for applications where the output voltage may vary over a wide range as may be the case with USB-PD (5 V 20 V) and Quick Charge (5 V 20 V); may not be required for fixed output voltage applications.

SZ1110 PRODUCT BRIEF

# **Product Ordering Information Note 1**

Part Number	Package	Feature	Shipping Method
SZ1110-00	16-pin SOIC	Hiccup Mode Fault Protection (All Faults)	5,000 pcs Tape & Reel
SZ1110-02	16-pin SOIC	Hiccup Mode Fault Protection (OTPs Latched)	5,000 pcs Tape & Reel
SZ1110-03	16-pin SOIC	Latched Mode Fault Protection (UV Auto-Recovery)	5,000 pcs Tape & Reel

#### Note:

16-pin package with two pins removed.

## **Package Dimensions**

	COMMON	DIMENSION			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM		
Α	-	-	1.75		
A1	0.10	-	0.25		
A2	1.30	-	1.50		
b	0.33	-	0.51		
b1	0.21	-	0.48		
С	0.19	-	0.25		
c1	0.10	-	0.23		
D	9.80	-	10.01		
E	5.80	-	6.20		
E1	3.84	-	3.99		
е	1.27 BSC				
e1					
L	0.51	_	0.76		
L1					
θ	0 degree	-	8 degree		
θ1	7 degree REF				
aaa	0.10				
bbb	0.20				
eee	0.10				
N	14 (16-2)				

- NOTE:

  1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994
  2. DIMENSIONS IN MILLIMETERS (ANGLES IN DEGREES)
  3. DIMENSION S IN MILLIMETERS (ANGLES IN DEGREES)
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCED 0.15mm PER END. D AND E1 DIMENSIONS ARE DETERMINED AT THAT DATUM H.

  4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSION D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

  5. DATUMS A & B TO BE DETERMINED AT DATUM H.

  6. THE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 TO 0.25mm FROM THE LEAD TIP.

  7. THE CHAMFER FEATURE IS OPTIONAL IF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED

  8. DIMENSION "5" DOES NOT INCLUDE THE DAMBAR PROTUSION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

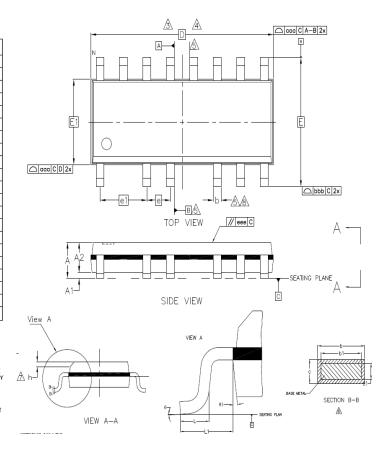


Figure 5: Package Dimensions

Silanna Semiconductor Proprietary and Confidential Information furnished by Silanna Semiconductor is believed to be accurate and reliable. However, no responsibility is assumed for its use. Silanna Semiconductor makes no representation that the

interconnection of its circuits as described herein will not infringe on existing patents rights.

