Silanna Semiconductor | Power Management Re-Imagined

SZPB9314A-B

15 V, 25 A, HIGH PERFORMANCE HALF BRIDGE

Features

- *ZqFET*™ High Performance Technology
- Supports Switching Frequencies up to 2 MHz
- $R_{DS(ON)4.5V}$ of 9 / 2.4 mΩ (Q1 / Q2)
- Extremely Low Gate Charge and Output Capacitance for Low Switching Losses
- QFN 5.1 mm x 4mm Thermally Enhanced Package

Applications

- Small, Efficient DC/DC Converters
- Battery Powered Electronics
- Power Blocks for Buck or Buck-Boost Converters

Product Description

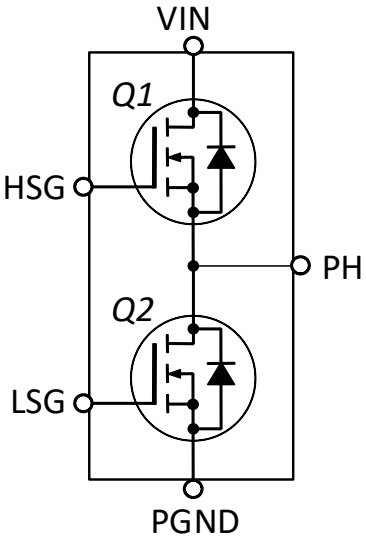
The SZPB9314A-B is a compact, high efficiency half bridge optimized for high frequency applications. It contains Silanna's proprietary *ZqFET*™ in a half bridge configuration, capable of delivering 25 A of output current with a wide range of inputs up to 15 V.

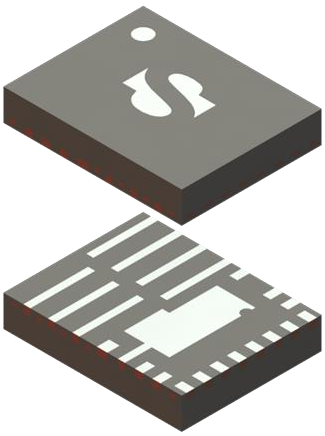
Silanna's proprietary *ZqFET*™ technology offers industry's benchmark performance that reduces both switching and conduction losses for operation at switching frequencies up to 2 MHz.

The SZPB9314A-B has been optimally designed for operation as a half bridge for high frequency DC/DC buck converters. The device is fabricated in a standard silicon process. The *ZqFET*™ structure provides for extremely low, world class switching losses for a given on resistance rivalling devices fabricated in exotic processes.

The SZPB9314A-B is available in a space-saving and thermally enhanced QFN 5.1 mm x 4 mm package.

Device Overview





WARNING: *These devices have limited built-in ESD protection. The leads should be shorted together with the device placed in conductive containers during storage or handling to prevent electrostatic damage to the Power ZqFET®'s MOS gates.*

Contents

Figures

Pin Descriptions

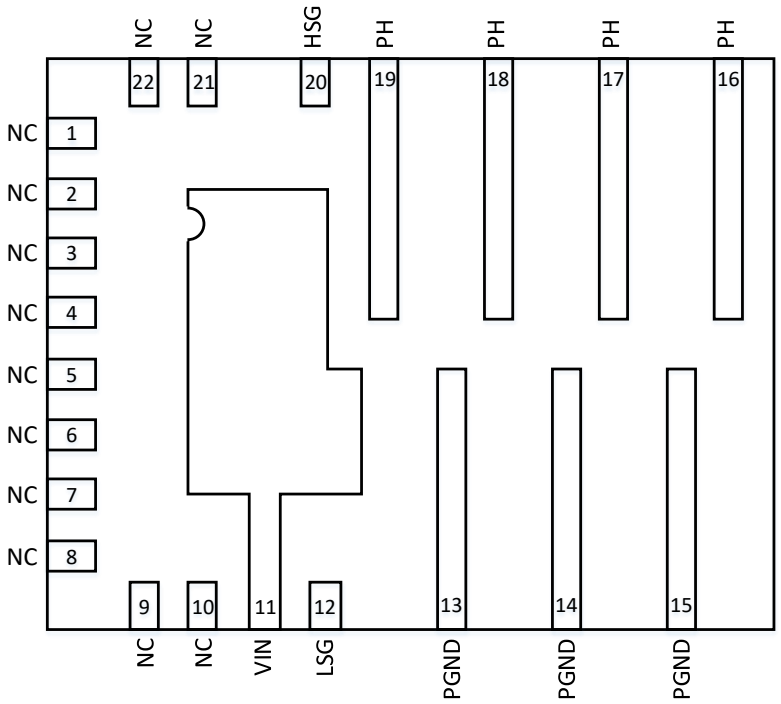


Figure 1: Top Transparent View

Pin Definitions

Pin #	Name	Description
1-10	NC	No connect. May be used to connect to a large PCB pad area of VIN.
11	VIN	Input voltage to Power Block, drain of Q1.
12	LSG	Input connection to the gate of the low-side FET, Q2.
13-15	PGND	Power ground connection to the source of the low-side FET, Q2.
16-19	PH	Connections to the phase node of the half bridge, drain of low-side FET and source of the high-side FET.
20	HSG	Input connection to the gate of the high-side FET, Q1.
21-22	NC	No connect. May be used to connect to a large PCB pad area of VIN.

Internal Block Diagram

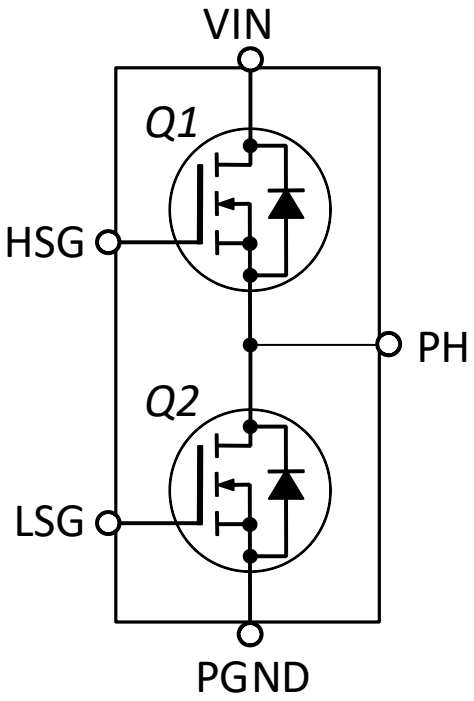


Figure 2: Internal Block Diagram

Absolute Maximum Ratings Note 1

(Ta = 25°C unless otherwise specified, relative to PGND.)

Parameter	Symbol	Device	Value	Units
Gate-Source Voltage	Vgs	Q1	9.0	V
		Q2	9.0	
VIN Voltage	Vvin		18.0	V
PH Voltage, DC	Vphase_dc		18.0	V
PH Voltage, AC (<10 ns)	Vphase_ac		25.0	V
DC Drain-Source Current (Tj = 150 °C)	Id	Q1	20	A
		Q2	25	
Pulsed Drain-Source Current (2)	Idm	Q1	30	A
		Q2	38	
Operating Junction Temperature	Tj	BOTH	-40/+150	°C
Storage Temperature	Ts	BOTH	-50/+150	°C

Notes:

1) These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to conditions greater than Recommended Operating Conditions will affect device reliability.
2) Pulse width ≤ 1ms, duty cycle ≤ 2%.

Thermal Information Note 1

Parameter	Symbol	Typ.	Units
Thermal Resistance Junction to Ambient	$R_{\Theta JA}$	25.7	°C/W
Thermal Resistance Junction to Top of Package	$R_{\Theta JC(TOP)}$	8.7	
Thermal Resistance Junction to Board	$R_{\Theta JB}$	4.8	
Thermal Characterization Parameter - Junction to top	Ψ_{JT}	0.2	
Thermal Characterization Parameter - Junction to board	Ψ_{JB}	4.8	

Notes:
1) Simulated on 2S2P JEDEC 51-7 board.

Recommended Operating Conditions

(Ta = 25°C unless otherwise specified.)

Parameter	Symbol	Conditions		Max.	Units
VIN Operating Voltage (1)	V_{VIN}	Insure any ringing on PH pins does not exceed Absolute Maximum ratings for PH pins.		15	V
Gate-Source Operating Voltage	V_{GS}		BOTH	5.5	V
Operating Frequency (2)	F_{SW}			2	MHz
Operating Junction Temperature	T_J			-40/+125	°C

Notes:
1) Attention to proper VIN supply bypassing and tight PCB layout must be observed to keep the peak voltage of any ringing on the phase node, at the PH pins, below the **Error! Reference source not found.**above.
2) The device is very capable of switching at higher frequencies. Contact Silanna with your requirements so we can best ensure the highest reliability for the device in your applications at higher switching frequencies.

Static Electrical Characteristics

(Ta= 25°C Unless Otherwise Specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Gate-Source Leakage Current	Igss	Vds = 0 V, Vgs = +5.5 V			10	100	nA
		Vds = 0 V, Vgs = -5.5 V		-100	-10		
Gate-Source Threshold Voltage	Vth	Vgs = Vds, Id = 250 µA	Q1	0.85	0.97	1.15	V
			Q2	0.70	0.91	1.10	
Drain-Source Breakdown Voltage	Bvdss	Vgs = 0V, Id = 250 µA	Q1	25			V
			Q2	25			
Drain-Source Leakage Current	Idss	Vds = 12.5 V, Vgs=0	Q1		125	1000	nA
		Vds = 12.5 V, Vgs=0	Q2		400	2000	
Drain-Source On-State Resistance (4.5 V)	$R_{DS(ON)4.5V}^{(1,2)}$	Vgs = 4.5 V, Id = 20 A	Q1		8.6	12	mΩ
		Vgs = 4.5 V, Id = 25 A	Q2		2.4	3.6	

Notes:

1) Measured using pulse techniques – pulse width = 300 µs and duty cycle = 1% to minimize junction self-heating.
2) Measured using 4-wire (Kelvin) voltage sensing within 0.05” (2 mm) of the drain and source aggregate connections.

Dynamic Electrical Characteristics

(Ta= 25°C unless otherwise specified)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Gate-Source Input Capacitance(2)	Ciss	Vds = 12.5 V, Vgs = 0 V, f = 1.0 MHz	Q1		630	800	pF
			Q2		2160	2400	
Drain-Source Output Capacitance(2)	Coss	Vds = 12.5 V, Vgs = 0 V, f = 1.0 MHz	Q1		560	750	pF
			Q2		2100	2400	
Reverse Transfer (Drain-Gate) Capacitance	Crss	Vds = 12.5 V, Vgs = 0 V, f = 1.0 MHz	Q1		13		pF
			Q2		47		
Gate Resistance	Rg		Q1		0.4		Ω
			Q2		0.8		
Total Gate Charge (Vgs = 4.5 V) (2)	Qg(4.5)	Vds = 12.5 V, Ids = 20 A	Q1		4.1	5	nC
		Vds = 12.5 V, Ids = 25 A	Q2		14.4	18	
Threshold Gate Charge(1)	Qg(th)	Vds = 12.5 V, Ids = 20 A	Q1		0.83		nC
		Vds = 12.5 V, Ids = 25 A	Q2		2.98		
Gate-Source Charge	Qgs	Vds = 12.5 V, Ids = 20 A	Q1		1.44		nC
		Vds = 12.5 V, Ids = 25 A	Q2		5.16		
Gate-Drain (Miller) Charge	Qgd	Vds = 12.5 V, Ids = 20 A	Q1		0.46		nC
		Vds = 12.5 V, Ids = 25 A	Q2		1.64		
Output Charge	Qoss	Vds = 12.5 V, Ids = 20 A	Q1		8.3		nC
		Vds = 12.5 V, Ids = 25 A	Q2		29.7		

Notes:

1) Qg(th) is defined as the gate charge value to the measured value of the gate-source threshold voltage, Vgs(th).
2) Guaranteed by characterization, not 100% production tested.

Product Ordering Information

SZPB9314A-BF54	15 V, 25 Amp Half Bridge in a 5.1 mm x 4 mm, 0.5 mm lead pitch, 22 lead QFN

Product Image

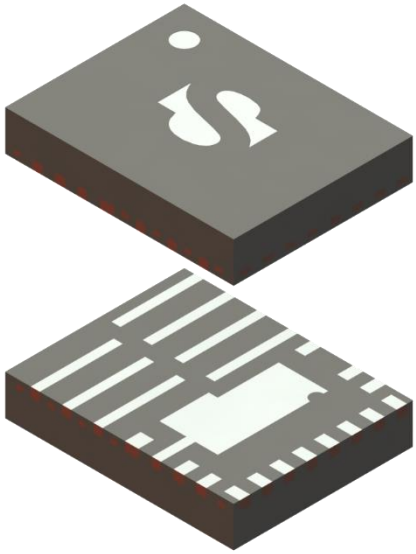
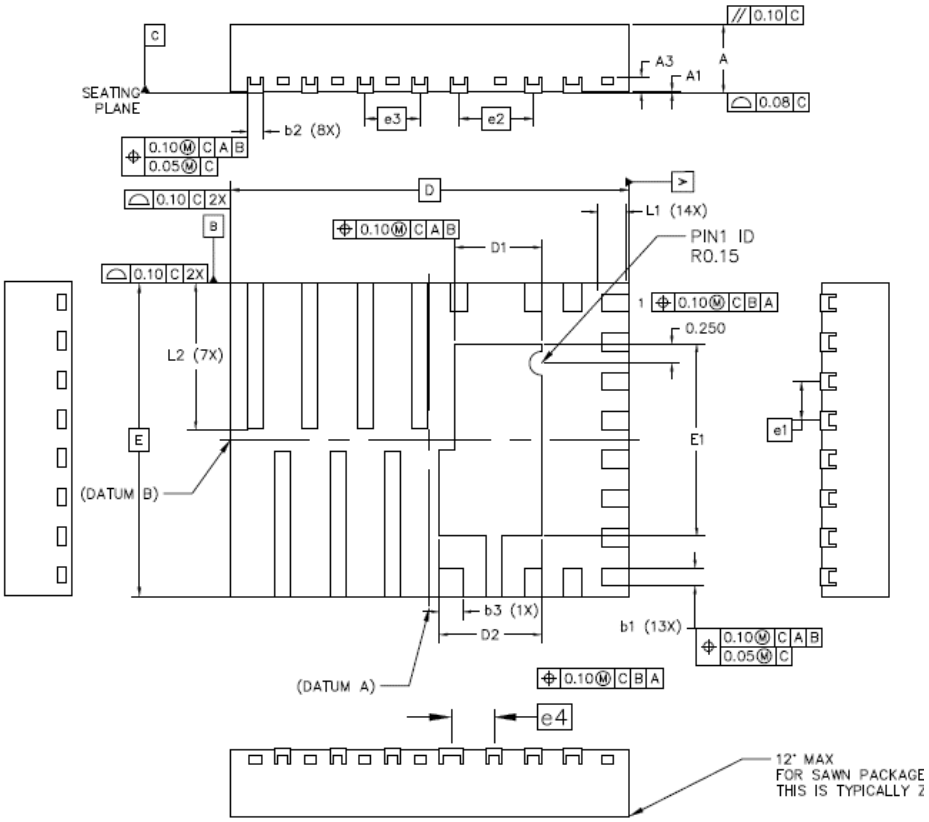


Figure 3: SZPB9314A-B Product Image

Package Dimensions



DIMENSION TABLE			
SYMBOL	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF	
b1	0.18	0.23	0.28
b2	0.15	0.20	0.25
b3	0.25	0.30	0.35
D		5.10 BSC	
E		4.00 BSC	
D1	1.00	1.10	1.20
D2	1.20	1.30	1.40
E1	2.36	2.46	2.56
e1		0.50 BSC	
e2		0.95 BSC	
e3		0.70 BSC	
e4		0.55 BSC	
L1	0.25	0.35	0.45
L2	1.77	1.87	1.97
N		22	

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5–2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Unilateral coplanarity zone applies to the exposed pas as well as the terminals

Figure 4: F54 Package Dimensions

Recommended PCB Footprint

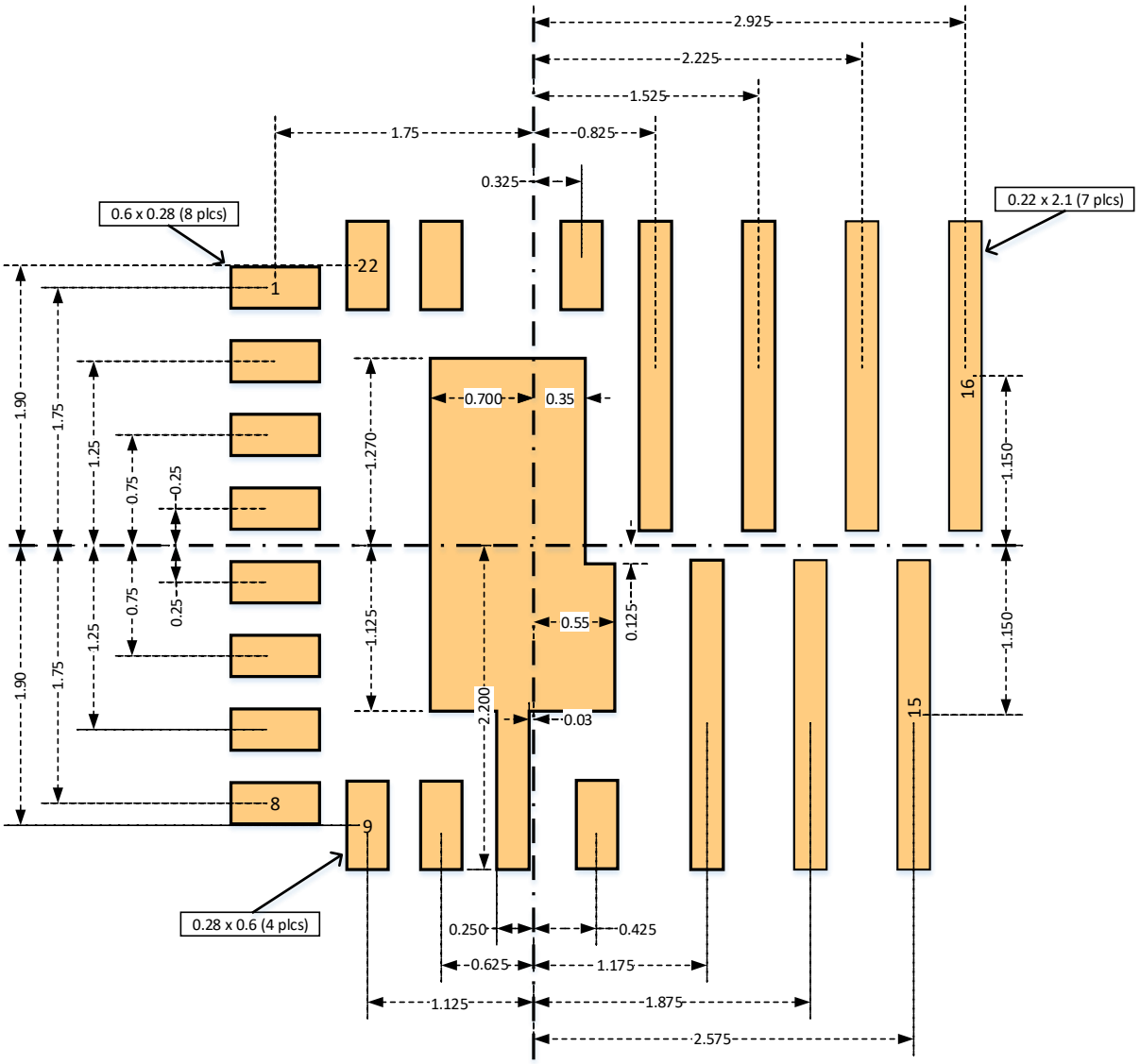


Figure 5: Recommended PCB Footprint

Revision History

Date	Revision	Notes	Author
June 18, 2018	1.0	Initial release	TW
October 7, 2018	2.0	Corrected figure 1. Updated Thermal Information, Static Electrical Characteristics, and Dynamic Electrical Characteristics. Final release.	TW
March 11, 2019	3.0	Update hyperlinks.	CR
June 20, 2019	4.0	Update header/footers and add the new logo.	CR

4795 Eastgate Mall, Suite 100, San Diego, CA 92121
Toll Free: (888) 637-3564 | Fax: (858) 373-0437 | www.powerdensity.com