Silanna Semiconductor | Power Management Re-Imagined

# SZPB9317A-B

## 15 V, 8 A, HIGH PERFORMANCE HALF BRIDGE

## Features

- *ZqFET*™ High Performance Technology
- Supports Switching Frequencies up to 2 MHz
- $R_{DS(ON)4.5V}$ of 20 / 8 mΩ (Q1 / Q2)
- Extremely Low Gate Charge and Output Capacitance for Low Switching Losses
- QFN 3.7 mm x 4 mm Thermally Enhanced Package

## Applications

- Small, Efficient DC/DC Converters
- Battery Powered Electronics
- Power Blocks for Buck or Buck-Boost Converters

## Product Description

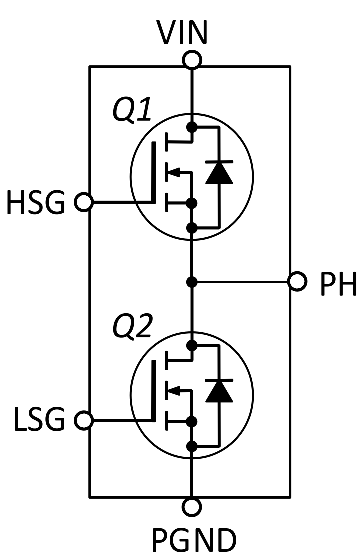
The SZPB9317A-B is a compact, high efficiency half bridge optimized for high frequency applications. It contains Silanna's proprietary *ZqFET*™ in a half bridge configuration, capable of delivering 8 A of output current with a wide range of inputs up to 15 V.

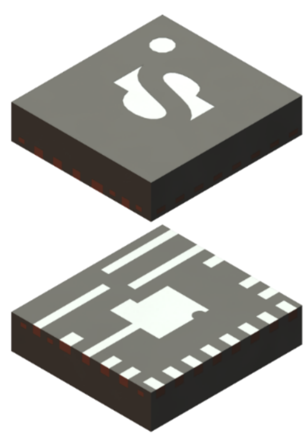
Silanna's proprietary *ZqFET*™ technology offers industry's benchmark performance that reduces both switching and conduction losses for operation at switching frequencies up to 2 MHz.

The SZPB9317A-B has been optimally designed for operation as a half bridge for high frequency DC/DC buck converters. The device is fabricated in a standard silicon process. The *ZqFET*™ structure provides for extremely low, world class switching losses for a given on resistance rivalling devices fabricated in exotic processes.

The SZPB9317A-B is available in a space-saving and thermally enhanced QFN 3.7 mm x 4 mm package.

## Device Overview



**WARNING**: *These devices have limited built-in ESD protection. The leads should be shorted together with the device placed in conductive containers during storage or handling to prevent electrostatic damage to the Power ZqFET®'s MOS gates.*

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# Pin Descriptions

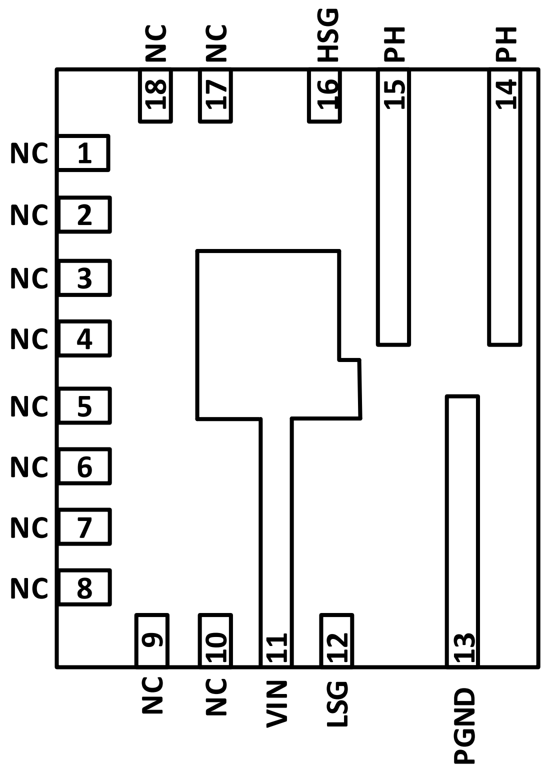



**Figure 1: Top Transparent View**

# Pin Definitions

| Pin # | Name | Description |
|---|---|---|
| 1-10 | NC | No connect. May be used to connect to a large PCB pad area of VIN. |
| 11 | VIN | Input voltage to Power Block, drain of Q1. |
| 12 | LSG | Input connection to the gate of the low-side FET, Q2. |
| 13 | PGND | Power ground connection to the source of the low-side FET, Q2. |
| 14-15 | PH | Connections to the phase node of the half bridge, drain of low-side FET and source of the high-side FET. |
| 16 | HSG | Input connection to the gate of the high-side FET, Q1. |
| 17-18 | NC | No connect. May be used to connect to a large PCB pad area of VIN. |

## Internal Block Diagram

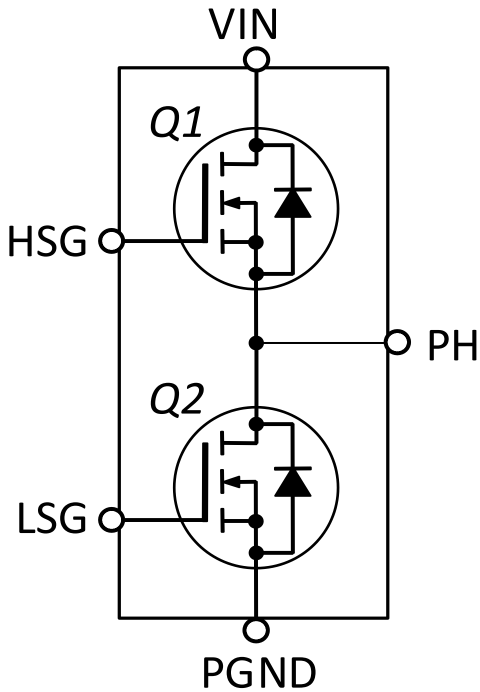



**Figure 2: Internal Block Diagram**

## Absolute Maximum Ratings Note 1

(Ta = 25°C Unless Otherwise Specified, relative to PGND.)

| Parameter | Symbol | Device | Value | Units |
|---|---|---|---|---|
| Gate-Source Voltage | Vgs | Q1 | 9.0 | V |
| | | Q2 | 9.0 | |
| VIN Voltage | Vvin | | 18.0 | V |
| PH Voltage, DC | Vphase_dc | | 18.0 | V |
| PH Voltage, AC (<10 ns) | Vphase_ac | | 25.0 | V |
| DC Drain-Source Current (Tj = 150 °C) | Id | Q1 | 8 | A |
| | | Q2 | 13 | |
| Pulsed Drain-Source Current (2) | Idm | Q1 | 12 | A |
| | | Q2 | 20 | |
| Operating Junction Temperature | Tj | BOTH | -40/+150 | °C |
| Storage Temperature | Ts | BOTH | -50/+150 | °C |

Notes:

1) These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to conditions greater than Recommended Operating Conditions will affect device reliability.
2) Pulse width ≤ 1ms, duty cycle ≤ 2%.

## Thermal Information Note 1

| Parameter | Symbol | Typ. | | Units |
|---|---|---|---|---|
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | Q1 | 30.1 | °C/W |
| | | Q2 | 31.7 | |
| Thermal Resistance Junction to Top of Package | $R_{\theta JC(TOP)}$ | Q1 | 14.7 | |
| | | Q2 | 15.9 | |
| Thermal Resistance Junction to Board | $R_{\theta JB}$ | Q1 | 6.6 | |
| | | Q2 | 8.3 | |
| Thermal Characterization Parameter - Junction to top | $\Psi_{JT}$ | 0.8 | | |
| Thermal Characterization Parameter - Junction to board | $\Psi_{JB}$ | 8.1 | | |

Notes:
1) Simulated on 2S2P board based upon JESD51-5 specifications.

## Recommended Operating Conditions

(Ta = 25°C Unless Otherwise Specified.)

| Parameter | Symbol | Conditions | Max. | Units |
|---|---|---|---|---|
| VIN Operating Voltage (1) | $V_{VIN}$ | Insure any ringing on PH pins does not exceed Absolute Maximum ratings for PH pins. | 15 | V |
| Gate-Source Operating Voltage | $V_{GS}$ | | 5.5 | V |
| Operating Frequency (2) | $F_{SW}$ | | 2 | MHz |
| Operating Junction Temperature | $T_J$ | | -40/+125 | °C |

Notes:
1) Attention to proper VIN supply bypassing and tight PCB layout must be observed to keep the peak voltage of any ringing on the phase node, at the PH pins, below the Absolute Maximum Ratings above.
2) The device is very capable of switching at higher frequencies. Contact Silanna with your requirements so we can best ensure the highest reliability for the device in your applications at higher switching frequencies.

## Static Electrical Characteristics

(Ta= 25°C Unless Otherwise Specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| Gate-Source Leakage Current | Igss | Vds = 0 V, Vgs = +5.5 V | | | 10 | 100 | nA |
| | | Vds = 0 V, Vgs = -5.5 V | | -100 | -10 | | |
| Gate-Source Threshold Voltage (ext) | Vth | Vgs = Vds, Id = 250 µA | Q1 | 0.9 | 1.0 | 1.2 | V |
| | | | Q2 | 0.75 | 1.0 | 1.2 | |
| Drain-Source Breakdown Voltage | Bvdss | Vgs = 0 V, Id = 250 µA | Q1 | 25 | | | V |
| | | | Q2 | 25 | | | |
| Drain-Source Leakage Current | Idss | VDS = 12.5 V, VGS=0 | Q1 | | 70 | 1000 | nA |
| | | VDS = 12.5 V, VGS=0 | Q2 | | 120 | 2000 | |
| Drain-Source On-State Resistance (4.5 V) | $R_{DS(ON)4.5V}$ (Notes 1,2) | Vgs = 4.5 V, Id = 8 A | Q1 | | 20 | 27 | mΩ |
| | | Vgs = 4.5 V, Id = 13 A | Q2 | | 8.5 | 11 | |
| Body Diode Forward Voltage | $V_{SD}$ | Vgs = 0 V, Id = 1 A | Q1 | | 0.72 | | V |
| | | | Q2 | | 0.69 | | |

Notes:

1) Measured using pulse techniques – pulse width = 300 µs and duty cycle = 1% to minimize junction self-heating.
2) Measured using 4-wire (Kelvin) voltage sensing within 0.05" (2 mm) of the drain and source aggregate connections.

# Dynamic Electrical Characteristics

(Ta= 25°C Unless Otherwise Specified)

| Parameter | Symbol | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| Gate-Source Input Capacitance | Ciss | Vds = 12.5 V, Vgs = 0 V, f = 1.0 MHz | Q1 | | 240 | 310 | pF |
| | | | Q2 | | 560 | 630 | |
| Drain-Source Output Capacitance | Coss | Vds = 12.5 V, Vgs = 0 V, f = 1.0 MHz | Q1 | | 210 | 280 | pF |
| | | | Q2 | | 500 | 600 | |
| Reverse Transfer (Drain-Gate) Capacitance | Crss | Vds = 12.5 V, Vgs = 0 V, f = 1.0 MHz | Q1 | | 5.5 | | pF |
| | | | Q2 | | 13.0 | | |
| Gate Resistance | Rg | | Q1 | | 0.3 | | Ω |
| | | | Q2 | | 0.5 | | |
| Total Gate Charge (Vgs = 4.5 V) | Qg(4.5) | Vds = 12.5 V, Ids = 8 A | Q1 | | 1.6 | 1.9 | nC |
| | | Vds = 12.5 V, Ids = 13 A | Q2 | | 3.9 | 4.5 | |
| Threshold Gate Charge (1) | Qg(th) | Vds = 12.5 V, Ids = 8 A | Q1 | | 0.30 | | nC |
| | | Vds = 12.5 V, Ids = 13 A | Q2 | | 0.76 | | |
| Gate-Source Charge | Qgs | Vds = 12.5 V, Ids = 8 A | Q1 | | 0.56 | | nC |
| | | Vds = 12.5 V, Ids = 13 A | Q2 | | 0.86 | | |
| Gate-Drain (Miller) Charge | Qgd | Vds = 12.5 V, Ids = 8 A | Q1 | | 0.16 | | nC |
| | | Vds = 12.5 V, Ids = 13 A | Q2 | | 0.33 | | |
| Output Charge | Qoss | Vds = 12.5 V, Ids = 8 A | Q1 | | 3.1 | | nC |
| | | Vds = 12.5 V, Ids = 13 A | Q2 | | 7.5 | | |

Notes:

1) Qg(th) is defined as the gate charge value to the measured value of the gate-source threshold voltage, Vgs(th).

## Product Ordering Information

| | |
|---|---|
| SZPB9317A-BF34 | 15 V, 8 Amp Half Bridge in a 3.7mm x 4 mm, 0.5 mm lead pitch, 18 lead QFN package. |

## Product Image

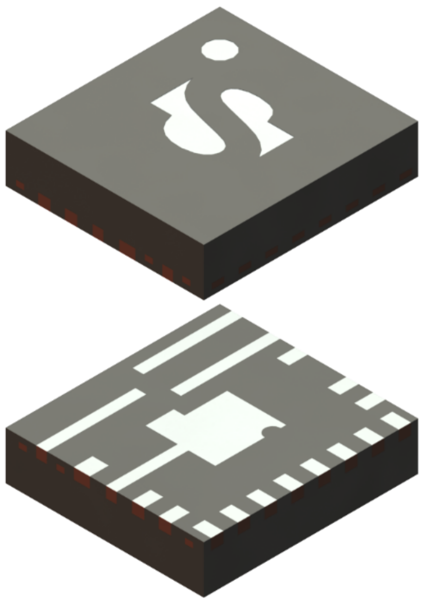
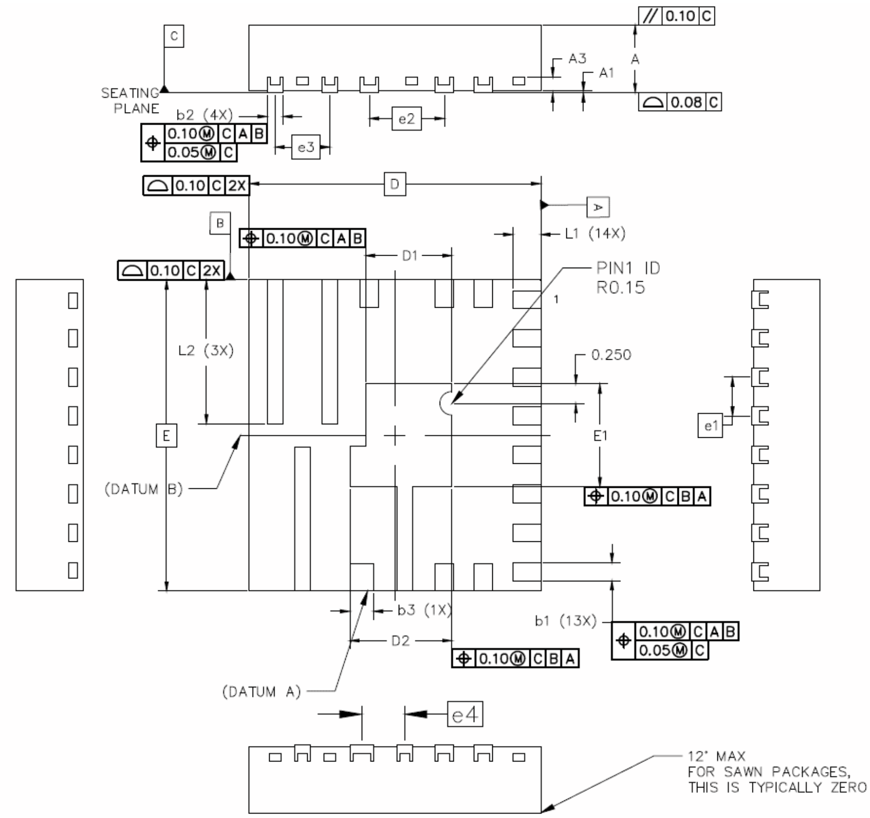


**Figure 3: SZPB9317A-B Product Image**

# Package Dimensions




| DIMENSION TABLE | | | |
|---|---|---|---|
| SYMBOL | MINIMUM | NOMINAL | MAXIMUM |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 Ref | |
| b1 | 0.18 | 0.23 | 0.28 |
| b2 | 0.15 | 0.20 | 0.25 |
| b3 | 0.25 | 0.30 | 0.35 |
| D | | 3.70 BSC | |
| E | | 4.00 BSC | |
| D1 | 1.00 | 1.10 | 1.20 |
| D2 | 1.20 | 1.30 | 1.40 |
| E1 | 1.22 | 1.32 | 1.42 |
| e1 | | 0.50 BSC | |
| e2 | | 0.95 BSC | |
| e3 | | 0.70 BSC | |
| e4 | | 0.55 BSC | |
| L1 | 0.25 | 0.35 | 0.45 |
| L2 | 1.77 | 1.87 | 1.97 |
| N | | 18 | |

NOTE:
1. Dimensioning and tolerancing conform to ASME Y14.5–2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Unilateral coplanarity zone applies to the exposed pas as well as the terminals

**Figure 4: F34 Package Dimensions**

# Recommended PCB Footprint

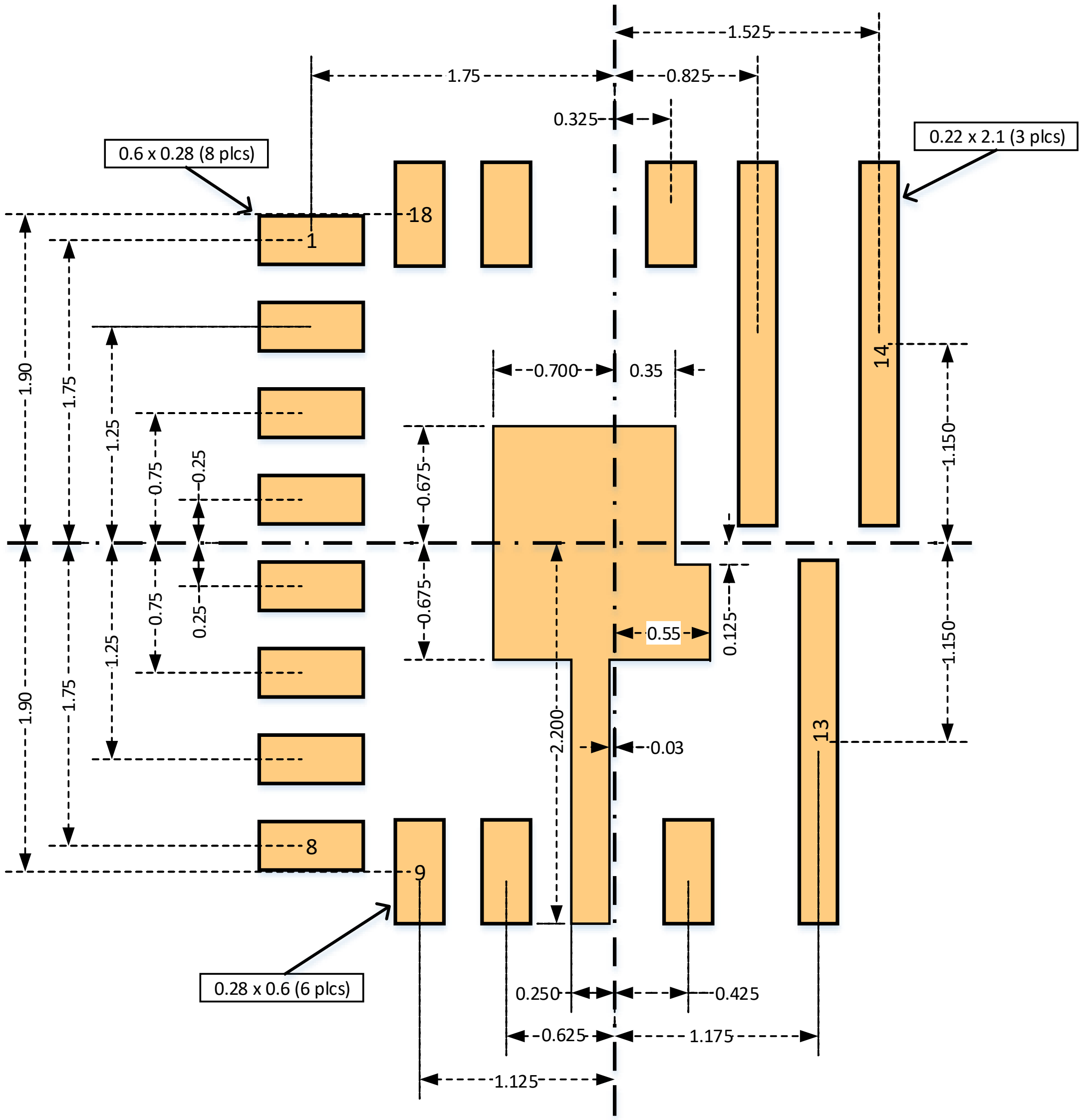



Figure 5: Recommended PCB Footprint

# Revision History

| Date | Revision | Notes | Author |
|---|---|---|---|
| June 18, 2018 | 1.0 | Initial release | TW |
| August 21, 2018 | 2.0 | Adjusted Thermal Information specs. | TW |
| March 12, 2019 | 3.0 | Final Datasheet release. | TW |
| June 20, 2019 | 4.0 | Update header/footers and add the new logo. | CR |



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