Silanna Semiconductor | Power Management Re-Imagined

Senior Test Engineer

Type: Full-time
Reports To: **Director of Test Engineering**
Location: San Diego, CA

Silanna designs and produces a family of Power Management IC's including high efficiency power stages and controller point of load solutions supporting applications from enterprise servers to telecom, wireless charging, USB-PB, industrial DC/DC, AC/DC, power modules etc. The person best suited for this role will have strong experience developing and deploying production test solutions for analog mixed signal power devices using commercial ATE platforms and automated bench solutions to support characterization. Essential duties and responsibilities include but are not limited to:

- Work with Silanna Design teams to establish test plans and to incorporate design for testability.
- Team up with Silanna product and test engineers to develop test hardware and software solutions needed to support product characterization, qualification and volume production. Leverage Silanna's commercial ATE. Silanna maintains Eagle 364 and FTI test platforms on-site as well as production class wafer probe systems.
- Develop bench solutions to support ATE correlation and to augment characterization.
- Build test platforms tuned for ease of re-use to optimize quick-turns of derivative products.
- Guarantee test solutions are stable by running appropriate gauge R&R and characterization.
- Optimize test solutions for best throughput and lowest cost without compromising quality.
- Follow Silanna standards to release and sustain test solutions at off-shore facilities.

Qualifications and Education Requirements

- Minimum BSEE with 8+ years in test and manufacturing of Power or analog mixed signal products.
- Demonstrated track record developing and deploying high volume production test solutions. (Millions of units)
- Demonstrate a thorough understanding of design for testability as it relates to analog, mixed signal and power products. Provide examples of your influences on DFT.
- Knowledge of competitive test cost structure and volume throughput constraints in production.