

Senior Staff Functional Verification Engineer

Type: Full-time
Reports To: Director of Design
Location: San Diego, Toronto or Raleigh

As part of a small, fast moving, innovation focused company, the Senior Staff Functional Verification Engineer will work closely with analog / mixed signal design engineers to define, create and verify Verilog-ams and/or System Verilog models for analog, mixed signal and power conversion circuits in order to improve chip level AMS simulation time and coverage. The engineer will also work with the mixed signal, digital and systems engineers to define the mixed signal and digital simulation test benches (including regression), then assist with running and analyzing simulation results and debugging AMS simulation issues using Cadence tools. A self-driven engineer is needed who can troubleshoot a range of simulation issues and continuously improve simulation coverage and speed.

Experience:

- 10+ years professional experience in modeling and mixed signal simulation of analog and mixed signal IC designs

Core competencies and responsibilities:

- In-depth technical knowledge of Verilog-AMS and system verilog
- Strong knowledge of analog/mixed signal integrated circuit fundamentals and core cells on analog ICs (power management knowledge a plus)
 - Develop models that accurately represent analog circuit behaviors
- Proficient in Cadence mixed signal simulation tools (synopsis digital design tool knowledge a plus)
 - create chip level functional verification testbenches, then work with mixed signal team to run and analyze results
 - compare model behavior to transistor level circuits (when available) and document model performance/specifications
- Verilog/VHDL language knowledge required
- Scripting skills required (Perl, Python, TCL or other)
- create clear model definitions/documentation and communicate to design engineers in multiple locations
- Able to thrive in a team-oriented environment with engineers in multiple locations