Silanna Semiconductor | Power Management Re-Imagined

SZDL3105B-A

High Voltage, High Efficiency, 100W Buck Converter

Features

- 667 kHz Switching Frequency
- Optimal High Efficiencies for 3.3 V to 21 V Vout
- Maximum Output Current of 5 A
- Wide Input Voltage Range: 7 V to 27 V
- Selectable Soft Start Times
- OCP/OVP/OTP Protections
- Programmable UVLO
- 4 mm x 4 mm QFN Package

Applications

- VBUS Supply Generation for USB-PD Ports:
  - Multiple Output USB-PD Chargers
  - Charging Hubs
  - Displays and Televisions
  - Laptop Docking Stations

Product Description

The SZDL3105B is a fully integrated high efficiency synchronous buck DC/DC converter intended to be paired with USB port controllers. The device is optimized for the highest efficiency performance, including dual input LDOs for self-bias, across a wide output voltage range.

The SZDL3105B is designed to supply the full range VBUS rail for USB-PD SPR ports and can be controlled by popular USB-PD controllers or fast charging devices. On start-up, the device employs an internal feedback path to allow safe regulation until the external PD controller powers up and becomes available to regulate the output voltage. Following this initial start-up period, the SZDL3105B hands over output control to the external PD controller.

The SZDL3105B is available in a compact 4 mm x 4 mm custom QFN package, delivering high power density with a minimal number of external components.

Application Diagram

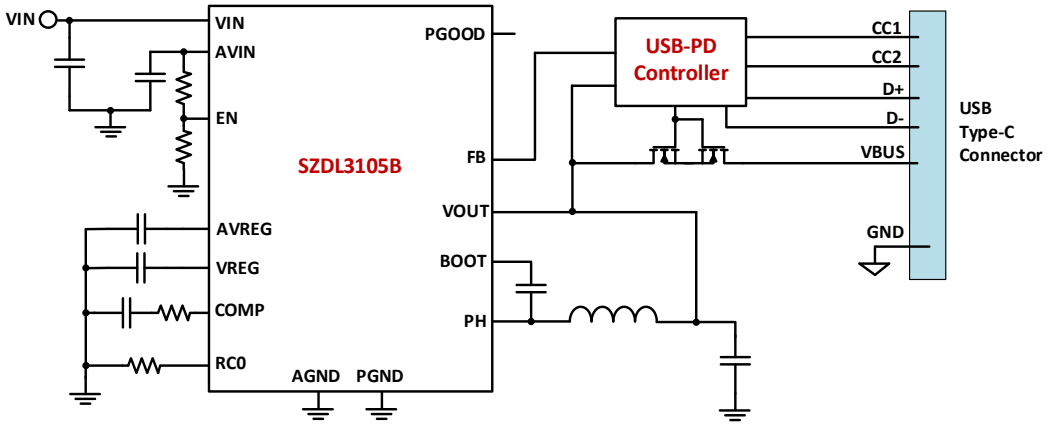

Figure 1. Typical SZDL3105B USB-PD Port Application Diagram

Package Pinout

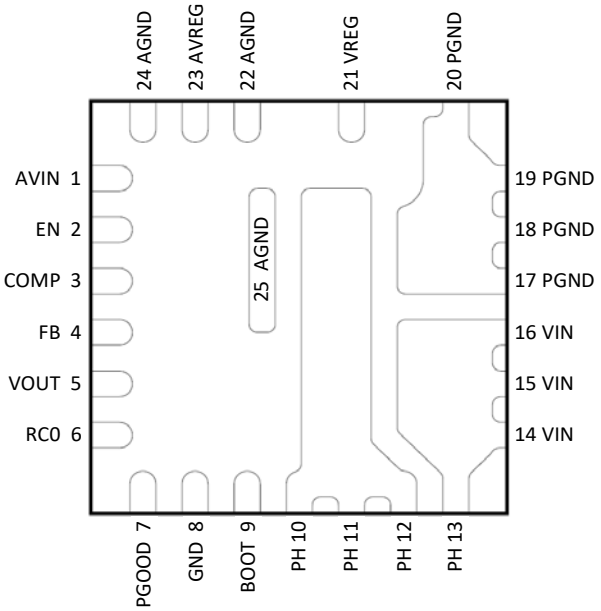

Figure 2. Package Pinout - Top View

Pin Definitions

Pin #	Name	Description
1	AVIN	Input voltage to the buck converter for analog circuits, internally derived from and matching VIN amplitude. Connect to an effective minimum 1 µF bypass capacitor to ground.
2	EN	Analog control input. A potential higher than the UVLO threshold enables switching operation and output soft start process. A potential lower than the shutdown threshold places the device in a low power state. To ensure proper initialization, the EN pin voltage should transition between the shutdown (V_{EN_SDH}) and UVLO thresholds (V_{EN_UVLO}) no faster than 1.8 ms. Decouple with a high quality ceramic capacitor of at least 10 nF placed close to the device. See the Functional Description paragraph for a more detailed explanation of its operation.
3	COMP	Compensation error amplifier output. Connect to RC network to ground. See the Applications Information section for recommendations.
4	FB	Feedback input pin, nominally regulated to 1.25 V. Connect to the tap of a VOUT-to-AGND resistor divider network (if needed by the USB port controller device) and the analog feedback control output of a USB port controller device.
5	VOUT	Voltage sense line from regulated output of converter and secondary input to internal LDOs.
6	RC0	Analog input. A resistor to ground sets the soft start time (t_{SS}).
7	PGOOD	Power good output signal. Active high, open drain output. Connect to pullup resistor to VREG.
8	GND	Connect to ground.
9	BOOT	Bootstrap high side driver voltage supply. Connect to 0.1 µF capacitor to PH node.
10-12	PH	Phase (switch) node of the buck converter's output FETs. Connect to output inductor.
13-16	VIN	Input voltage to the buck converter's output FETs (high side drain). Locally decouple with 1 µF + 0.1 µF capacitors, followed by sufficient capacitors to provide required input RMS current.
17-20	PGND	Power ground connection of output FETs (low side source). Connect to ground.
21	VREG	Internal 3.45 V LDO output. Connect to an effective minimum 2.2 µF bypass capacitor to ground.
22,24,25	AGND	Connect to ground.
23	AVREG	Internal 3.4 V LDO output. Connect an effective minimum 2.2 µF bypass capacitor to ground.

Functional Block Diagram

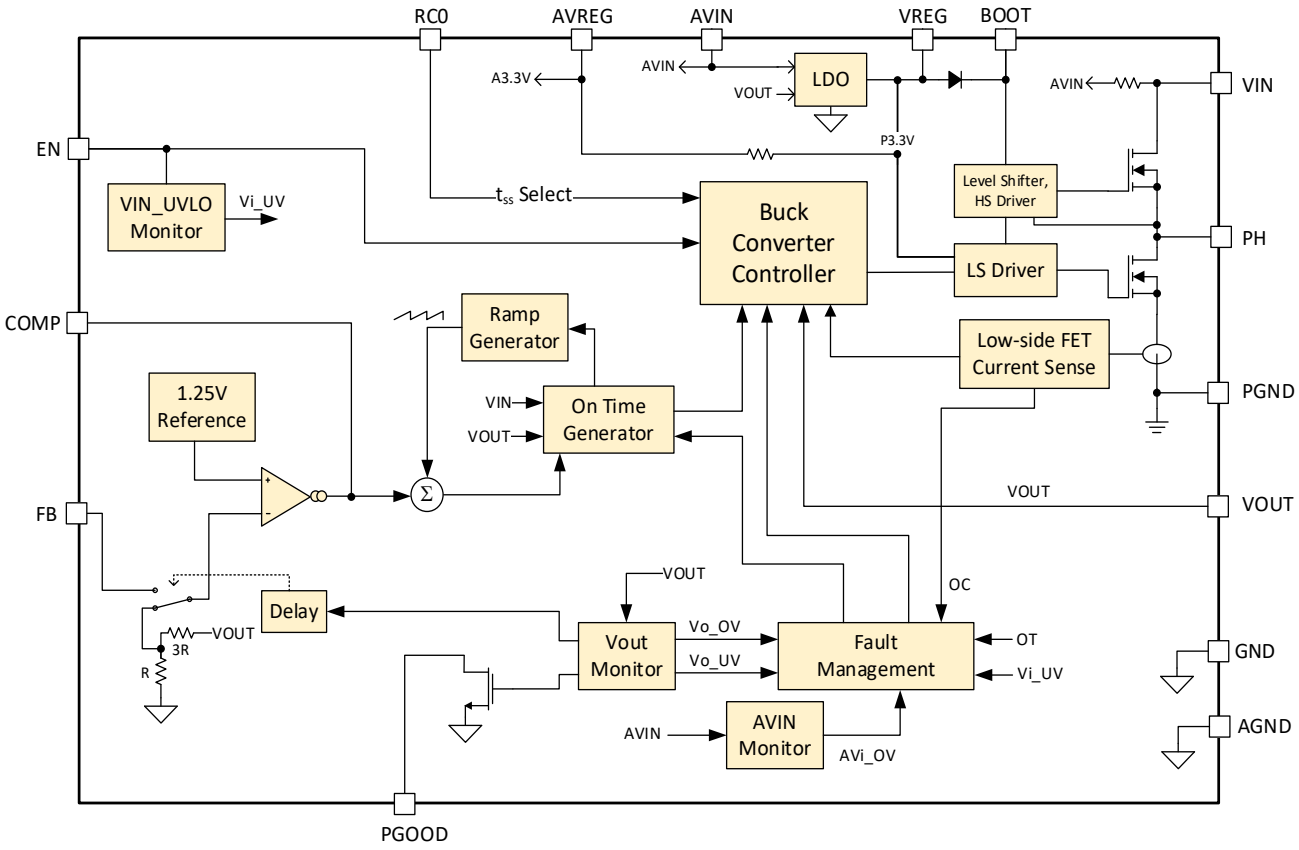

Figure 3: Functional Block Diagram

Product Ordering Information

Part Number	Package	Description
SZDL3105B-AQXC	QFN (4 mm x 4 mm)	100 W, USB-PD Buck Converter; with internal FB divider at power up

Product Image

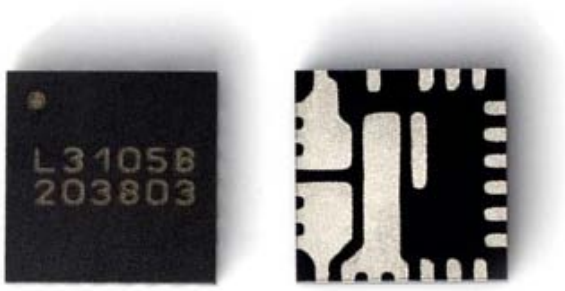

Figure 4: SZDL3105B Product Image

Revision History

Revision	Date	Author	Note
1.0	07/15/2021	TW	Initial Release.
2.0	09/20/2021	TW	Edited EN pin description of rise time.

4795 Eastgate Mall, Suite 100, San Diego, CA 92121
Toll Free: (888) 637-3564 | Fax: (858) 373-0437 | www.SilannaSemi.com