# EMI Management: Design, Layout and Mitigation

## Introduction

Customers develop their reference designs to meet EMI specifications per Industry standards. This Application note will assist customers in meeting their EMI requirements by providing design and layout guidance during the Design phase and by providing mitigation guidance during the Validation phase in case it's needed.

There are multiple sections in this App note as follows:

- Industry Specifications
- Design & Layout w/ EMI in mind
- Component Placement
- Return Path and Routing
- Resistor & Capacitor Component Selection
- Magnetic Components Design
- Thermal Mitigation and its Impact
- Improving performance or Mitigating Issues

## Industry Specifications

Figure 1 shows an example radiated emissions signature, and the Class B specification limits are illustrated with the red line for a 3-meter chamber. The horizontal (x-axis) ranges from 30MHz to 1GHz.

| Frequency Range (MHz) | Quasi Peak (dBµV/m) |
|---|---|
| 30 – 230 | 40 |
| 230-1000 | 47 |

**Table1: Radiated Emissions Limits (Class B)**

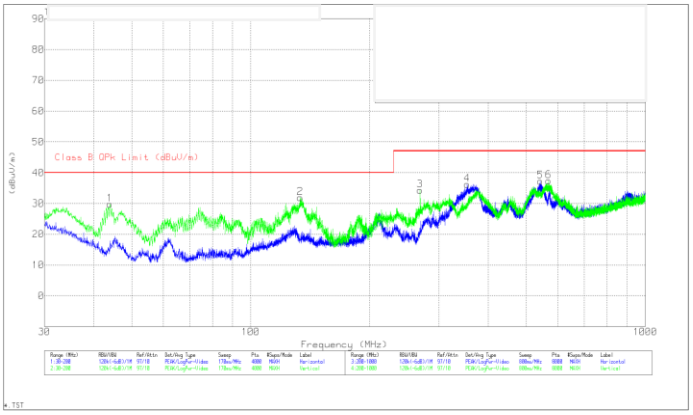



**Fig 1: Example Radiated Emissions Graph (3-meter Class B)**

Figure 2 shows an example conducted emissions signature, and the Class B specification limits are illustrated with the red line for Quasi-Peak and the blue line for Average. The horizontal (x-axis) ranges from 150KHz to 30MHz. The specs are also shown in the Table2 following the graph.

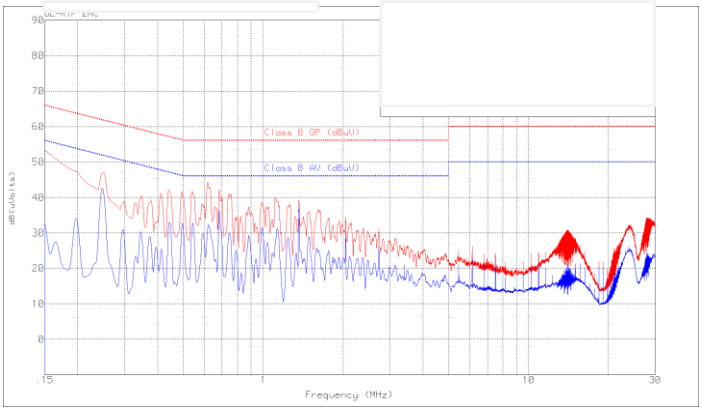



**Fig 2: Example Conducted Emissions Graph**

| Frequency Range (MHz) | Quasi Peak (dBµV) | Average (dBµV) |
|---|---|---|
| 0.15 – 0.5 | 66 to 56 | 56 to 46 |
| 0.5 - 5 | 56 | 46 |
| 5 - 30 | 60 | 50 |

**Table2: Conducted Emissions Limits (Class B)**

### Margin Beyond the Specs

Due to lab-to-lab variations and board-to-board variations, customers require new designs to have margin beyond the specs so that the probability of finding a unit that doesn't meet the specifications is very low. Customer's margin requirements vary but 6dB, 4dB or 3dB below the spec are common.

This Application Note will use a Multi-Port Charger Reference Design which includes one of our Active Clamp Flyback converters for the AC/DC stage followed by two of our DC/DC buck converters to drive the two USB Type-C ports

## Design & Layout w/ EMI in mind

As with any significant development, creating a design to meet your requirements is usually less costly and time-consuming than addressing major issues afterward. Therefore, care should be taken in the Design and Layout of reference designs by considering resistor and capacitor component selection, magnetic component's design, beads and CMCs component selection, component placement, power & signal loops' size and return paths and grounding

### Magnetic Components Design

#### Transformers

Transformer design & construction have a significant impact on EMI. Manufactured Transformers are preferred but hand winding is acceptable when employing skilled personnel. Belly bands are recommended, and they should be grounded to the primary side Bulk Ground. Also, utilize shield winding(s) between the primary side winding and secondary side winding interfaces using the same number of turns as secondary. Utilize parallel strands to fill the entire bobbin window. Thinner wires are preferred in order to achieve lower leakage inductance. Note, that this method is not always give the expected improvement therefore several iterations is needed. See the reference designs' transformer spec sheet for details.

#### CMCs

Design/select CMCs based on common-mode and differential noise attenuation curves. They should attenuate frequencies of interest the most. If common-mode noise is not dominant a differential inductor can be utilized. Also, ferrite or nanocrystalline (10k) is desired.

### Resistor & Capacitor Component Selection (AC/DC)

#### Primary FET (Rgate & RC snubber)

The ACF's primary switch turn-on should be slowed down to achieve <-5V/ns drain-to-source slew-rate either via Rgate or Rconfig which allows the user to configure the amount of current used to slew the gate up and down. This will eliminate ringing on SR FET and may eliminate the need for SR FET snubber. There is no efficiency impact since zero-current switching occurs during turn-on. 5V/ns number is a rule-of-thumb; it may be quite different depending on the transformer design (leakage inductance). An R-C snubber across the Drain-to-Source of the primary FET, however, is an important tool for managing Radiated EMI and we recommend designs include provisions to support this in case it's needed during design validation. Primary switch turn-off can be slowed down if radiated EMI is problematic due to turn-ff. Cds values between 33pF and 100pF typically deliver a few to several dB of reduction. Resistor values of 2 to 4 ohms typically help further by dampening ringing due to parasitic inductance. Take care when choosing the component values because they will reduce efficiency.

#### Y Capacitor

The Y capacitor value should be maximized where possible. A value between 470-2200pF are recommended but designs have been demonstrated with one tenth as much Y-cap. Two Y-capacitors will improve margin a few dB more than a single Y-capacitor. They should be terminated to different points, such as VBULK-SGND, PGND-SGND. Care shall be taken to comply with IEC62368

#### X Capacitor

The X capacitor value and the bleeding resistor should be maximized according to allowable no-load power consumption. For the designs using the SZ1131

- <20mW = 47nF
- <30mW = 150nF
- <75mW = 470nF

Noted that comply with IEC62368 is needed

#### HV Bulk Capacitors

HV Ceramic capacitors (10-47nF) should be added in parallel with bulk electrolytic capacitors to filter high frequency noise

#### Auxiliary Diode Snubber

An RC snubber of 33ohms and 100pF across the auxiliary diode can also reduce radiated emissions

## Resistor & Capacitor Component Selection (DC/DC)

### Phase Snubber

An optional R-C snubber on the Phase node can me a useful tool to manage emissions from the DC/DC buck converter. Our reference designs don't need this RC snubber to pass but it can be a good option if you're having difficulty meeting spec with your design. R=10hms and C=220pF is a good place to start but take care in selecting value since they will reduce efficiency.

### Boot Resistor

An optional resistor can also be a useful tool to manage emissions from the buck converter. A nominal value of 10ohms is typical with a typical window of 5 to 15 ohms. Our reference designs don't need the boot resistor to pass but it can be a good option if you're having difficulty meeting spec with your design.

### Vin-Vout Capacitor

A 22nF Vin-Vout capacitor is recommended to deliver improved radiated emissions by providing a tightly coupled transient source of energy when the high side is turning on.

### Vin Decoupling capacitors

Take care when selecting the capacitor values and the case sizes for Vin decoupling since they provide the source of current for the converter during transitions. Including 0402, 0603 and 1206 capacitors with expected lower parasitic inductance delivers emissions improvements. Maximize the self-resonant frequency of the capacitor where possible to ensure it acts like a capacitor at the highest frequency possible.

### Vin Decoupling at Daughter Card Transitions

In multi-port designs Daughter cards are often employed due to shape requirements. This can lead to DC/DC converters that are not on the same board as the AC/DC part whose output feeds the input to the DC/DC. It is strongly recommended, when power is routed from the AC/DC board to the DC/DC board, that decoupling capacitors be added at the card edge. This is important when managing emissions. A similar mindset should be employed if a long power supply route is required on board. That should be avoided, but if it is required, intermediate Vin decoupling is also recommended.

## AC/DC Layout Guidelines

### Minimize power Loops (AC/DC)

The first priority is to minimize the loop area and the 2nd priority is to minimize length. See the text descriptions followed by the image shown in Figure 3

- BULK HF_cap => Primary transformer winding => ACF Primary FET
- Clamp_cap => Primary transformer winding => ACF Internal FET
- VOUT HF_cap => ACF Secondary Side FET => Secondary transformer winding

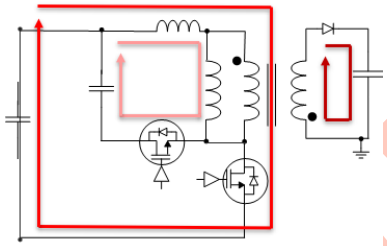


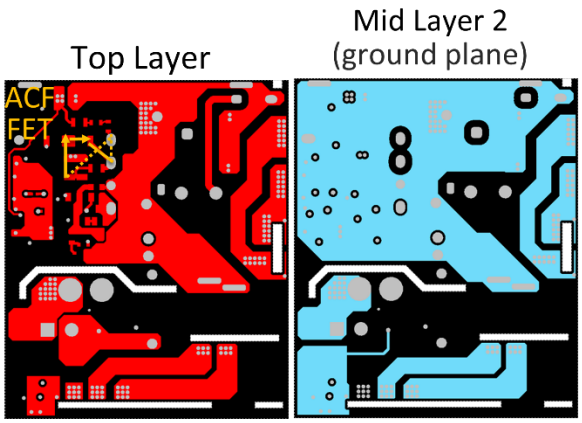
**Fig 3: Key AC/DC Loops**

### Primary Side Switch

A surface mount switch delivers better EMI performance than a through-hole switch. It also often works better thermally.

## AC/DC Layout Layers with tight Loops (Fig4)

- Ground plane utilized for RE shielding as well as to allow for minimization of HF power loops
- Note that ground plane is placed under SZ1131 as well as Primary ACF-FET
- E-caps utilized as shield between ACF and input filter/AC as well as secondary side/DC-DC
- Tight power loops (RED main ACF FET loop, GREEN secondary ACF FET loop, ORANGE ACF FET loop)



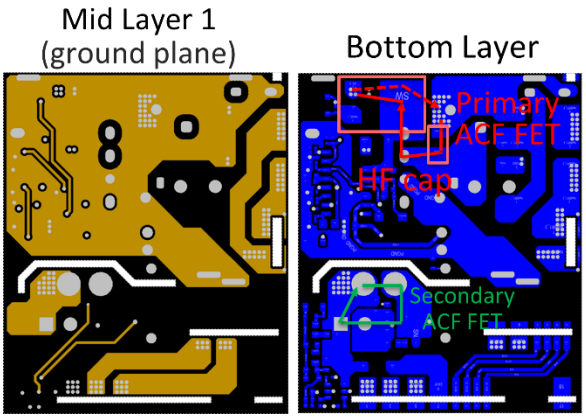



**Fig 4: AC/DC Tight Layout Loops Illustrated**

### Component Placement (AC/DC)

Component placement is critical for decoupling. See the text descriptions followed by the image shown in Figure 5

- Utilize ACF Bulk capacitors as a shield between ACF and Input Filter/AC side
- Utilize ACF Bus capacitor as shield between ACF and secondary side/DC-DC

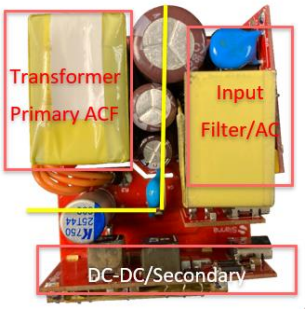



**Fig 5: AC/DC Component Placement**

### Ground Plane (AC/DC)

- Place a ground plane under all high-frequency paths to minimize RE, especially SZ1131/ACF Primary FET/Clamp capacitor
- Fill-in all planes as much as possible
- Keep away from input filter/AC side to reduce parasitic coupling

Leverage proven designs and use recommended layouts where possible when creating new designs

## DC/DC Layout Guidelines

### Minimize power Loops (DC/DC)

The first priority is to minimize the loop area and the 2nd priority is to minimize length. See the text descriptions followed by the image shown in Figure 6

- VIN =>HS-FET(Q1) =>Phase =>Vout_Cap =>GND =>Vin_Cap =>Vin
- GND =>LS-FET(Q2) =>Phase =>Vout =>Vout_Cap =>GND

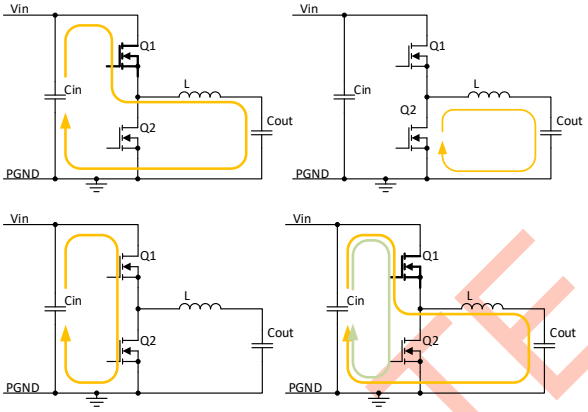



**Fig 6: DC/DC Loops**

## DC/DC Layout Layer with tight Loops (Fig7)

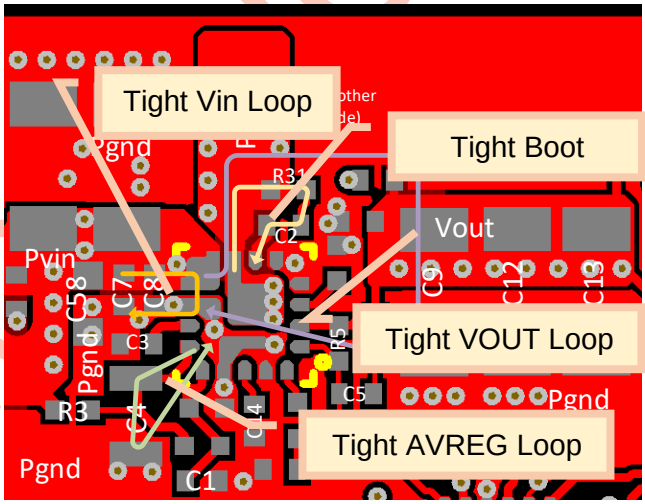



**Fig 7: DC/DC Tight Layout Loops Illustrated**

### Component Placement (DC/DC)

Component placement is critical for decoupling

- Place the IC next to the edge of any Board-to-Board connections to minimize the Vin route length from the AC/DC to the DC/DC.
- Decoupling capacitors closest to the IC on Vin, Vreg/Vdd, BST and Vout in that priority order
- Decoupling capacitors placed at the edge of any Board-to-Board connections especially power.

### Ground Plane (DC/DC)

- Breaks in the ground plane should be minimized. Take care to understand the return path of the key, high-speed lines and eliminate breaks under them. This will manage the fields emitted and help keep them as small as possible
- Fill GND Copper on all planes, but maintain isolation between noisy and quiet sides of any beads or CMCs used

### Board Layers (AC/DC & DC/DC)

- Don't put signal layers between Power and ground
- Power and ground should be on adjacent layers
- Signals can be combined with Power and Ground
- Every signal is a max of 1 dielectric away from power or ground

### Thermal Management and EMI

As output power levels continue to rise, despite improvements in efficiency, thermal heat spreaders are often employed to manage the surface temperature of the cases by reducing hot spots. When they're made of metal, care must be taken to not create an antenna and potentially introduce an emission source. Heat sinks should be grounded in multiple locations to suppression emissions. Care must also be taken when using heatsinks that couple from one region to another that were deliberately kept isolated. The presence of this large heatsink can degrade EMI performance. It's better, in that instance, to use separate heat sinks.

## EMI Improvement or Mitigation

### Debug

It can be beneficial to both test the AC/DC and DC/DC boards together and separately to help isolate the root cause. Care should be taken because the boards when together can have mutual benefits that could be lost when separated. Once the source of emissions is identified, confirm the layout and components follow best practices.

#### Conducted EMI

- <500kHz
  - Increase differential inductance
  - Increase X-capacitance value (if possible)
- 500kHz-30MHz
  - Shield primary switch and/or transformer windings from rest of circuit with copper grounded foil
  - Increase Y-capacitance value (if possible)
  - Add a grounded shield over the IC and the phase node or even better over the entire DC/DC board
- >10MHz
  - Slow-down primary switch turn-off
  - Add RC snubber on secondary side FET
  - Add small CMC to the input filter (2 or 3T)

#### Radiated EMI

- 30-50MHz
  - Slow-down primary switch turn-off
  - Add RC snubber on secondary side FET
  - Add small CMC (2-5T)
- 80-300MHz
  - Slow down primary switch turn-off
  - Shield primary switch and/or transformer windings from rest of circuit with copper grounded foil
  - Add ferrite bead on primary switch or transformer windings with high impedance at frequency of concern
  - Add small CMC (2-5T)
- >200MHz
  - Reduce Y-capacitance or add ferrite bead on Y-capacitor (ideally, low-Z at CE freq range)
  - Add a Phase snubber and/or a boot resistor on the DC/DC
  - Add a CMC or a High Current Bead in series with the output of the DC/DC (Vout)

#### CMCs & High Current Beads

Depending on the nature of the emissions you're trying to suppress, high current beads can be effective like CMCs, and yet are often smaller and cheaper. The key is ensuring the impedance is high at the frequency at which you're trying to suppress EMI.

## Additional Theoretical Comments

When we're designing to minimize EMI we're managing the Energy. The rate of change in the energy level with respect to time is what causes issues. At high-speed edge rates we use to deliver industry-leading performance, traces look like transmissions lines (distributed). They are no longer lumped. Thus, you have to pay close attention to the return path in addition to the source-outward path to properly minimize the fields and thus minimize EMI.

## References

[1] Morrison, Ralph. *Fast Circuit Boards: Energy Management*, Hoboken, NJ, Wiley, 2018

[2] Archambeualt, Bruce R. *PCB Design for Real-World EMI Control*. Norwell MA, Kluwer 2002

[3] Bogatin, Eric. *Bogatin's Practical Guide to Prototype Breadboard and PCB Design*, Norwood, MA, Artech House 2021

# Revision History

| Revision | Date | Author | Note |
|---|---|---|---|
| 0.1 | 10 Jul 2022 | DK | Draft release. |
| 1.0 | 09/10/2022 | HN | Initial release + Adding comment of IEC62368 and clarify some sections |
| | | | |