Application note AN1131 describes how to utilize Silanna's primary-side controller SZ1131 to design high power density active clamp flyback converters.

Introduction

The SZ1131 is an Active clamp Flyback (ACF) PWM Controller that integrates an adaptive digital PWM controller and the following Ultra High-Voltage (UHV) components: active clamp FET, active clamp driver and a start-up regulator.

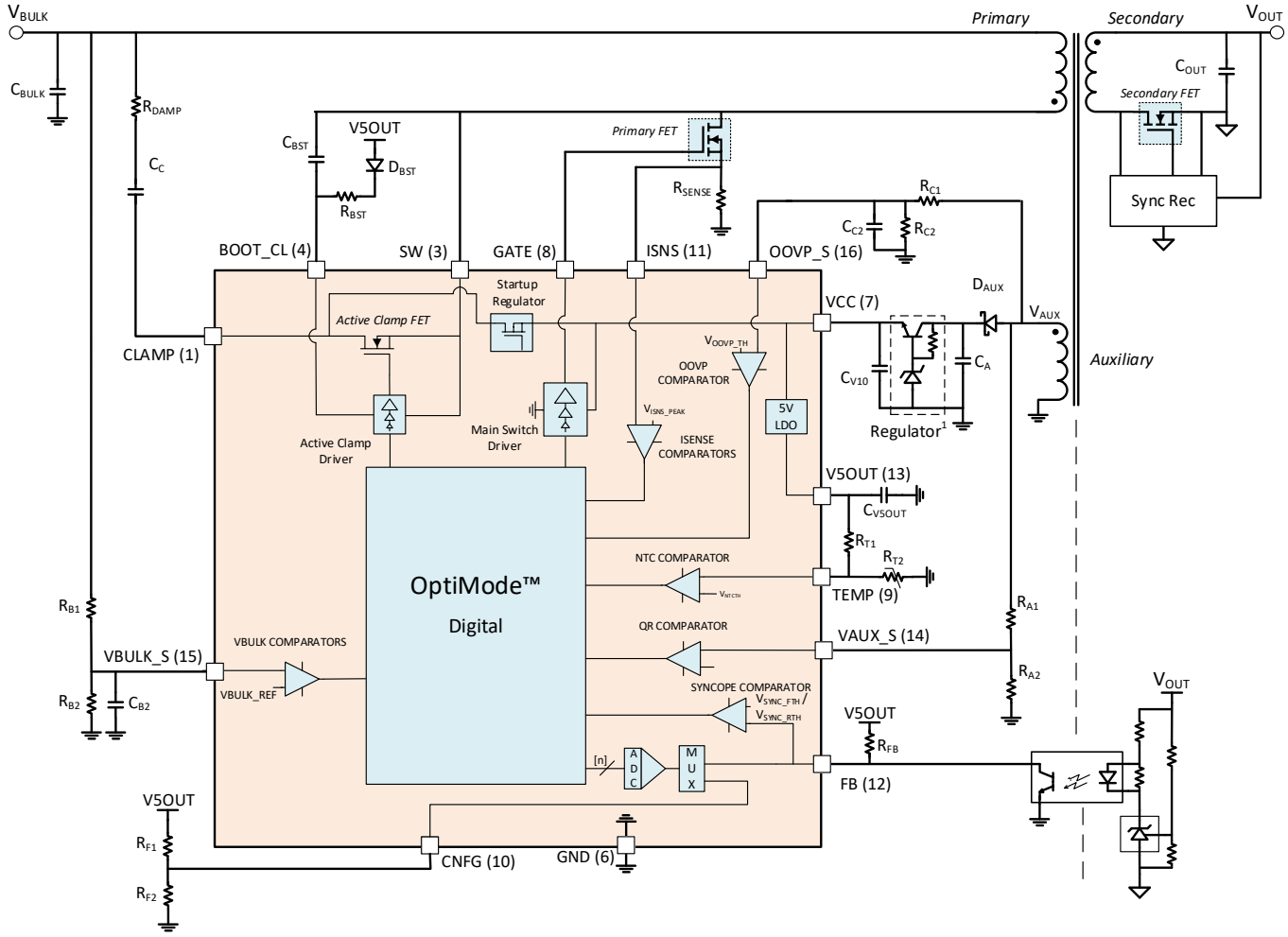

Figure 1: Typical Application Circuit of an Active clamp Flyback Converter using SZ1131

The device provides ease-of-design of a simple flyback controller with all the benefits of an ACF design, including recycling of the flyback transformer leakage energy and clamping of the primary FET drain voltage. Employing Silanna's OptiMode™ digital control architecture, the SZ1131 adjusts the device's mode of operation on a cycle-by-cycle basis to maintain high efficiency, low EMI, and fast dynamic load regulation.

Unlike conventional ACF designs, tight tolerances of the clamp capacitor and leakage inductance values are not required for proper operation of the circuit. Moreover, a small 3.3nF clamp capacitor is sufficient to realize the benefits of ACF operation. The SZ1131 is well suited for high efficiency and high-power density AC/DC power adapters.

Design Procedure

This section provides detailed step by step procedure for designing a flyback converter.

Input Power Calculation

Assuming over-current limit (OCL) allowance the maximum output power will be

$$P_{out}^{max} = P_{out} \cdot OCL$$

and the maximum input power as seen at the bulk capacitor is,

$$P_{in}^{max} = \frac{P_{out}^{max}}{\eta^{bulk}}$$

where η^{bulk} is the minimum efficiency of the converter from the bulk capacitor to the output capacitor, typically 94%.

Design Example – P_{max_out} for a typical 65W USB-PD adapter

The maximum output power is obtained using equation 1:

$$P_{out}^{max} = 65 \cdot 1.1 = 71.5W$$

The maximum input power is obtained using equation 2:

$$P_{in}^{max} = \frac{71.5W}{0.94} = 76W$$

Input Bulk Capacitor

Selection of input bulk capacitor largely depends on the supply mains of the region where the end product is intended for use. Shown in table **1** are the typical input voltage mains for various regions.

Country / Region	Input Voltage (VAC)	Nominal Line Frequency (Hz)
United States and Canada	90 – 132, 120 (Nom)	60
European Union and United Kingdom	185 – 265, 230 (Nom)	50
Japan	85 – 132, 100 (Nom)	50/ 60
China	185 – 265, 220 (Nom)	50
Korea	185 – 265, 220 (Nom)	60
Taiwan	90 – 265, 110 (Nom)	60

Table 1: Input AC mains voltage according to region

For low-line and universal AC line applications, bulk capacitance values equal to ~1.5uF per watt of input power are recommended while ~1uF per watt of input power is sufficient for high-line applications. These guidelines are used in order to maximize efficiency and provide sufficient stored energy for continuous operation during IEC-61000-4-11 type voltage sag events. For applications where low AC line operation requirements are relaxed (either in terms of maximum output power, efficiency, or voltage sag ride-through), the bulk capacitance values can be minimized.

For universal and low line applications, the recommended bulk capacitance value is :

$$C_{bulk} = 1.5 \cdot P_{in}^{max} uF$$

If the above recommendation is not followed it is imperative that the capacitance value be chosen such that the minimum bulk voltage, v_{bulk_min}, is greater than SZ1131 brown-out threshold (recommendation 75V). This can be calculated using the formulas below.

$$C_{bulk} > \frac{P_{in}^{max} \cdot (1 - D_{ch})}{f_{ac}} \cdot \frac{1}{2v_{ac\_min}^2 - v_{bulk\_min}^2}$$

where, v_{bulk_min} is the minimum input line voltage, P_{in}^{max} is the maximum input power, D_{ch} is the bulk capacitor charging duty ratio defined as shown in Figure 2: Input bulk capacitor voltage waveform

, C_{bulk} is the bulk capacitance, f_{ac} is the minimum AC line frequency.

The charging duty ratio, D_{ch} can be calculated as

$$D_{ch} = \frac{\frac{1}{4f_{ac}} - \frac{\sin^{-1}\left(\frac{v_{bulk\_min}}{\sqrt{2}\,v_{ac\_min}}\right)}{2\pi f_{ac}}}{\frac{1}{2f_{ac}}}$$

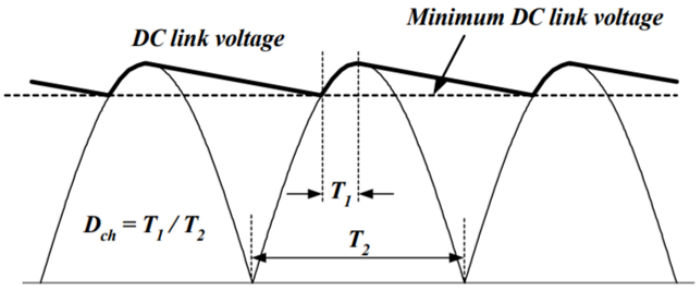

Figure 2: Input bulk capacitor voltage waveform

Design Example - C_{bulk} calculation for a typical 65W USB-PD adapter

Assuming converter specifications outlined in Table 1, D_{ch} & C_{Bulk} can be calculated using the above equations:

$$D_{ch} = \frac{\frac{1}{4f_{ac}} - \frac{\sin^{-1}\left(\frac{v_{bulk\_min}}{\sqrt{2}\,v_{ac\_min}}\right)}{2\pi f_{ac}}}{\frac{1}{2f_{ac}}} = \frac{\frac{1}{4\cdot 47} - \frac{\sin^{-1}\left(\frac{75}{\sqrt{2}\cdot 90}\right)}{2\pi\cdot 47}}{\frac{1}{2\cdot 47}} = 0.299$$

$$C_{bulk} > \frac{P_{in}^{max}\cdot(1-D_{ch})}{f_{ac}} \cdot \frac{1}{2v_{ac\_min}^2 - v_{bulk\_min}^2}$$

$$C_{bulk} > \frac{76\cdot 0.7}{47} \cdot \frac{1}{2\cdot 90^2 - 75^2} = 107uF\ (nominal) \approx 129\text{uF (20\% tolerance)}$$

For applications requiring greater than 75W output power, regulations require power factor correction which would necessitate the use of a front end converter to achieve active power factor correction. One of the most popular converters used for PFC is the boost topology. The boost topology will take its input from the rectified AC mains and will provide a boosted input to the active clamp flyback. For these cases, the boost output will be regulated to a certain voltage with corresponding output voltage ripple which will be the basis for the calculation of the input bulk capacitor.

Transformer Turns Ratio and Magnetizing Inductance

When the primary FET is off and the secondary side switch is conducting, the secondary side winding voltage is reflected on the primary winding. During this period, the primary FET drain and SZ1131 SW pin, V_{SW}, is exposed to a voltage approximately equal to reflected secondary winding voltage (V_{VOR}) plus the maximum bulk voltage (V_{bulk}). To ensure reliable operation of SZ1131 it is recommended that the maximum reflected secondary winding voltage, specifically the primary to secondary side transformer turns ratio, be selected in such a way that the primary FET peak drain and SW pin voltages are kept below 90% of the SZ1131 SW node maximum voltage rating, 620V at maximum rated input voltage.

The primary magnetizing inductance (L_M) can be bounded using,

$$L_M < \frac{(D_{max} \cdot V_{bulk\_min})^2}{2 \cdot P_{IN_{MAX}} \cdot PCL_{\Delta} \cdot f_{sw\_min}}$$

Where f_{sw_min} is the minimum converter switching frequency, PCL_{Δ} is the peak-current limit min-to-max variation (1.14) and D_{max} is the maximum primary side MOSFET duty cycle.

Design Example – *Turns ratio and magnetizing inductance* for a typical 65W USB-PD adapter

The maximum allowable voltage at the drain of the FET/SW pin is

$$V_{SW} = V_{SW}^{max} \cdot \text{derating factor} = 620V \cdot 0.9 = 558V$$

The maximum allowable reflected voltage, V_{VOR}^{max}, is given by the maximum allowable SW pin voltage, clamp capacitor AC voltage ripple (typically 40V, for more accurate estimate please refer to design tool) and maximum bulk voltage ($V_{AC}^{max} \cdot \sqrt{2}$),

$$V_{VOR}^{max} = V_{SW} - V_{AC\_CLAMP} - V_{bulk}^{max} = 558V - 40V - (265V_{RMS} \cdot 1.414) = 143V$$

The primary to secondary turns ratio can be calculated using the maximum allowable reflected voltage and maximum output voltage.

$$n = V_{VOR}^{max} / V_{out}^{max}$$

$$n = 143V / 20V = 7.2$$

During max duty-cycle operation it can be assumed that the flyback converter will be operating near boundary mode conduction and that the max duty cycle of the converter, D_{max}, is given by

$$D_{max} \approx V_{VOR} / (V_{bulk}^{min} + V_{VOR})$$

$$D_{max} \approx 143V / (75V + 143V) = 0.657$$

The minimum switching frequency is selected to be in the 40-60kHz range (lower frequency for optimized high-line efficiency and higher frequency for optimized low-line efficiency). The design tool can be utilized to provide a more accurate starting point for the design.

$$f_{sw\_min} = 55kHz$$

Substituting the values in the equation:

$$L_M < \frac{(0.657 \cdot 75)^2}{2 \cdot 76 \cdot 1.14 \cdot 55k} = 255uH$$

Primary Winding

The minimum number of primary turns (N_{P_min}) can be calculated using the formula :

$$N_{P\_min} = n\ x\ N_{S\_min}$$

Where n is the transformer turns ratio and N_{S_min} calculated as

$$N_{S\_min} = \frac{L_M \cdot I_{max}}{n \cdot B_{max} \cdot A_e} \cdot 10^6$$

where I_{max} is the maximum transformer primary current, A_e is the minimum equivalent magnetic core cross-sectional area in mm^2 and B_{max} is the saturation flux density in tesla at 120 deg C. An approximate value of Imax can be determined using the formula

$$I_{max} \approx \frac{2}{n} \cdot \frac{P_{in}^{max}}{V_{out}^{max}} \cdot \left(1.0 + \frac{D_{max}}{1 - D_{max}}\right)$$

Design Example – *Primary turns* for a typical 65W USB-PD Adapter (using ML29D RM8 core)

Primary/Secondary Turns Calculation

$$I_{max} \approx \frac{2}{n} \cdot \frac{P_{in}^{max}}{V_{out}^{max}} \cdot \left(1.0 + \frac{D_{max}}{1-D_{max}}\right) = \frac{2}{7} \cdot \frac{76}{20} \cdot (1.0 + \frac{0.657}{0.343}) = 3.08A$$

$$N_{S\_min} = \frac{L_m \cdot I_{max}}{n \cdot B_{max} \cdot A_e} x\ 10^6$$

$$N_{S\_min} = \frac{250H\ \cdot 3.08A}{7.2 \cdot 0.395T\ \cdot 55\ mm^2}\ x\ 10^6$$

L_m is chosen to be 250uH in order to allow N_{S_min} to be 5 turns.

$$N_{S\_min} = 5\ T$$

$$N_P = n \cdot N_S$$

$$N_P \geq 7.2 \cdot 5 = 36T$$

Primary Winding Wire diameter

The objective is to determine the appropriate wire diameter & number of strands so that copper losses (DC & AC resistance) are minimized. The first step is to determine the primary winding diameter. The primary winding diameter is calculated based on the skin depth to minimize the AC loss.

For the primary magnetizing current, which is a triangular shaped waveform, the major harmonics are the 1st and the 3rd.

Skin depth for the 3rd harmonic can be calculated as, $\delta = \sqrt{\frac{\rho}{\pi .\mu o .\mu r .f}}$

where,

ρ is the resistivity of the wire material (copper)

μ_o = permeability of free space

μ_r is the relative magnetic permeability of the wire material,

f is the frequency of interest.

Design Example – *Primary wire diameter* for a typical 65W USB-PD Adapter (using ML29D RM8 core)

Primary wire size calculation

$$\delta = \sqrt{\frac{2.3 \cdot 10^{-8}}{\pi \cdot 4\pi \cdot 10^{-7} \cdot 300k}} = 0.139mm$$

Assuming a fill factor of 90%, the maximum primary winding radius can be calculated as below:

$$\text{Fill factor} = \frac{(2 \cdot primary\ winding\ \ radius) \cdot \frac{N_p}{number\ of\ primary\ layers}}{Winding\_area\_length}$$

$$0.90 = \frac{(2 \cdot primary\ winding\ \ radius) \cdot \frac{36}{2}}{8.8}$$

Primary winding radius = 0.22 mm

Since the calculated skin depth δ is 0.139mm, the primary winding radius must be <0.139mm. Hence, two strands in parallel is required. So, the primary winding strand radius will be:

Primary winding radius = 0.22 / 2 = 0.11mm

The closest to that is AWG31 (0.113 mm).

Once the wire size is determined, it is a good practice to calculate the current capacity (circular mils per amp or CMA).

$$\text{Circular Mil per Amp , CMA} = \frac{CM\ of\ the\ winding \cdot No\ of\ parallel\ winding}{Irms}$$

For a nominal operating condition, V_{ac} = 90Vrms ,V_{out} = 20V, I_{out} =3.25A and C_{bulk} = 129uF, L_m = 250uH, N_p = 36T, N_s = 5T. The calculated primary I_{rms} value is ~1.13A.

$$\text{Circular Mil per Amp, CMA} = \frac{79.7 \cdot 2}{1.13} = 141.$$

The calculated CMA value is relatively lower than the nominal (200~500) range. It is advised to verify transformer temperature with an actual prototype.

Secondary Winding

It is advised to use a triple insulated wire for the secondary winding such to meet reinforced isolation between primary and secondary without additional insulation tape. Like the primary, secondary current waveform is also triangular. Hence considering major harmonics 1st and 3rd, the calculated skin depth is 0.139mm.

$$\text{Secondary winding wire diameter} = \left(\frac{Winding\ area\ length\ *FF}{Ns}\right)$$

Design Example – *Secondary wire diameter* for a typical 65W USB-PD Adapter (using ML29D RM8 core)

$$\text{Secondary winding wire diameter} = \left(\frac{Winding\ area\ length\ *Fill\ Factor}{Ns}\right)$$

Using the RM8 bobbin winding area length of 9.93 mm, we can calculate the wire diameter as :

$$Secondary\ winding\ wire\ diameter = \frac{9.93 * 0.9}{5} = 1.78\text{mm (0.07in)}$$

Since the calculated skin depth δ from our design example is 0.139mm, the constraint is that the strand OD has to be AWG31 or higher AWG. From the table below, TXXL360/44TXXX-3 (MWXX) can be selected since it is nominal OD is close to the theoretical calculations and meets the constraints.

PART NUMBER	EQUIV. AWG	CORE O.D. (in)	CIR. MILS	NO. STRANDS	AWG OF STRANDS	NOMINAL O.D.(in)
TXXL180/38TXXX-2(MWXX)	13.5	0.0694	2880	180	38	0.0814
TXXL180/38TXXX-3(MWXX)	13.5	0.0694	2880	180	38	0.0874
TXXL15/30TXXX-1.5(MWXX)	16.5	0.0485	1500	15	30	0.0575
TXXL15/30TXXX-2(MWXX)	16.5	0.0485	1500	15	30	0.0605
TXXL15/30TXXX-3(MWXX)	16.5	0.0485	1500	15	30	0.0665
TXXL360/44TXXX-2(MWXX)	15	0.0557	1440	360	44	0.0677
TXXL360/44TXXX-3(MWXX)	15	0.0557	1440	360	44	0.0737
TXXL19/36TXXX-2(MWXX)	21.5	0.0281	475	19	36	0.0401
TXXL19/36TXXX-3(MWXX)	21.5	0.0281	475	19	36	0.0461
TXXL35/38TXXX-2(MWXX)	21	0.0306	560	35	38	0.0426
TXXL35/38TXXX-3(MWXX)	21	0.0306	560	35	38	0.0486
TXXL07/30TXXX-1.5(MWXX)	20	0.0331	700	7	30	0.0421
TXXL07/30TXXX-2(MWXX)	20	0.0331	700	7	30	0.0451
TXXL230/44TXXX-2(MWXX)	17	0.0445	920	230	44	0.0565
TXXL230/44TXXX-3(MWXX)	17	0.0445	920	230	44	0.0625
TXXL40/40TXXX-1.5(MWXX)	22	0.0254	385	40	40	0.0344
TXXL40/40TXXX-2(MWXX)	22	0.0254	385	40	40	0.0374
TXXL07/32TXXX-1.5(MWXX)	21.5	0.0267	448	7	32	0.0357
TXXL07/32TXXX-2(MWXX)	21.5	0.0267	448	7	32	0.0387
TXXL19/40TXXX-1.5(MWXX)	25.5	0.0175	183	19	40	0.0265
TXXL19/40TXXX-2(MWXX)	25.5	0.0175	183	19	40	0.0295
TXXL05/32TXXX-1.5(MWXX)	23	0.0226	320	5	32	0.0316
TXXL05/32TXXX-2(MWXX)	23	0.0226	320	5	32	0.0346
TXXL16/44TXXX-1.5(MWXX)	30	0.0101	64	16	44	0.0191

Table 2: Wire Part Number and corresponding AWG & O.D value

Secondary Winding Wire Diameter

Corresponding CMA value of the secondary winding can be calculated as:

Circular Mil per Amp , CMA = $\frac{CM\ of\ the\ winding \cdot No\ of\ parallel\ winding}{Irms}$

Design Example – *Secondary wire diameter* for a typical 65W USB-PD Adapter (using ML29D RM8 core)

From the Table 4, the equivalent CMA value for the TXXL360/44TXXX-2 (MWXX) wire is 1440. For the same nominal operating condition (as used in the primary winding CMA), the secondary Irms current was calculated as ~ 5.83A.

Circular Mil per Amp, CMA = $\frac{1440 \cdot 1}{5.83}$ = 247

Core gap

With the determined turns of the primary side, the gap length of the core is obtained as

$$l_g \approx \mu_0 \frac{N_{pri} \cdot I_{max}}{B_{max}} \cdot \text{mm}.$$

Design Example – *Core gap* for a typical 65W USB-PD adapter

As only a minimal amount of energy is stored in the core itself, this factor may be ignored to simplify calculation.

$$l_g = 4\pi \cdot 10^{-7} \cdot \frac{36T \cdot 3.08A}{0.395T} = 0.35mm$$

Bias Windings

The recommended operating supply voltage of SZ1131 is from 7 V to 14.5 V. In most single output voltage power supplies, the supply to the VCC can be taken directly from a single auxiliary winding on the primary side of the transformer.

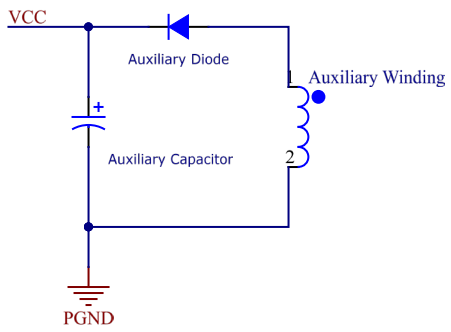

Figure 3: Direct bias auxiliary for standard single output applications

This winding is directly coupled to the secondary winding and the number of turns can be calculated using this formula :

$$Naux = \frac{(VCC_{nominal} + V_d)\ x\ N_{sec}}{V_{out\_min}}$$

Where Vcc_{typ} is the nominal Vcc voltage (8.1 V); N_{sec} is the number of secondary turns; Vd is the auxiliary diode forward voltage and V_{out_min} is the minimum output votatge during no load.

For applications where there are wide output voltage variations as in the case of battery chargers or for multiple output voltages for a single port such as USB-PD applcations, a two level bias winding is needed.

The design of the two-level bias winding, shown in Figure 8, starts with establishing the number of bias turns required for sufficient bias capacitor and *VCC* voltage during no-load.

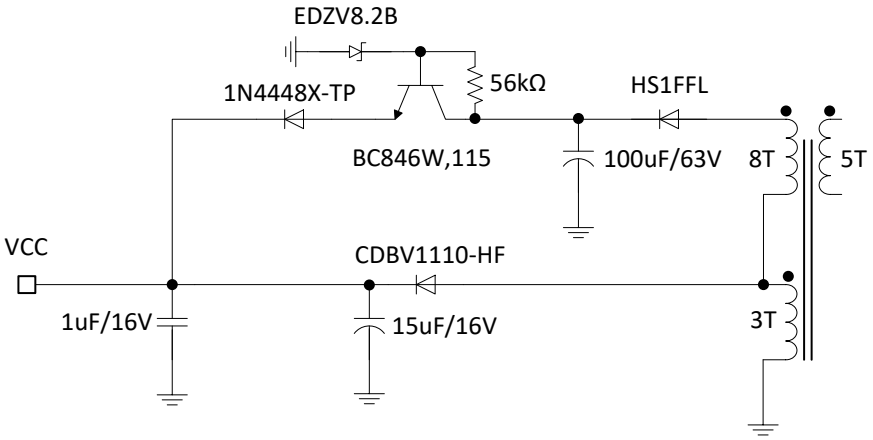

Figure 4: Dual-winding auxiliary regulator circuit for high performance USB PD applications

During no load operation the converter operates in burst mode. While in burst mode, the *VCC* pin voltage must be maintained above POR_{FALL_VCC} in order to guarantee that the internal UHV startup regulator remains off.

The minimum auxiliary winding voltage must be greater than POR_{FALL_VCC} plus the regulator drop (V_{LDO}), diode voltage (V_F) and auxiliary capacitor voltage ripple $V_{auxiliary\_ripple}$.

$$V_{aux} = POR_{FALL\_VCC} + V_{LDO} + V_F + V_{\text{auxiliary\_ripple}}$$

The minimum auxiliary winding turns (top+bottom winding combined) is then given by

$$N_{aux} > \left(\frac{N_{sec}}{V_{out\_min}}\right).\mathrm{V}_{aux}$$

Where N_{sec} is the number of secondary winding turns and V_{out_min} is the output voltage during no-load condition.

The maximum number of bottom auxiliary winding turns should be selected such that the maximum reflected voltage seen even in case of output over voltage is less than 15V.

$$N_{aux}^{bottom} < \left(\frac{N_{sec}}{1.2 \cdot V_{out\_max}}\right).15V$$

Design Example – *Bias winding turns and capacitance* for a typical 65W USB-PD adapter

Full auxiliary turns calculation

$$V_{aux} = 6.9V + 1.3V + 0.7V + 2V = 10.9\text{V}$$

$$N_{aux} \geq \left(\frac{N_{sec}}{V_{out\_min}}\right) \cdot V_{aux} \geq \frac{5T}{5V} \cdot 10.9\text{V} = 10.9\text{T}$$

Use 11T for N_{aux}.

$$N_{aux}^{bottom} < \left(\frac{N_{sec}}{1.2 \cdot V_{out\_max}}\right).15V = \frac{5T}{1.2 \cdot 20V} \cdot 15V = 3.1$$

Use 3T for N_{aux}^{bottom} and 8T for N_{aux}^{top}.

VCC and Bias Winding Capacitance

The VCC bias capacitance value is selected such that the stored energy can maintain the VCC voltage above the POR_{FALL_VCC} value until the auxiliary voltage is able to take over. The exact calcuation of this value is included in the design tool; however, for the purpose of this application note and it's intended scope the recommended value is in the 12-15uF range (effective value at 13V DC bias voltage and desired minimum operating temperature).

For applications with stringent no-load power requirements (<30mW) the $V_{auxiliary}$ capacitance value is selected such that the stored energy can support the transition to syncope mode of operation. The following equation can be used to estimate the required value

$$C_{aux}^{top} > \frac{i_{aux}^{light-load}}{i_{sec}^{light-load}} \cdot \frac{N_{sec}}{3 \cdot N_{aux}} \cdot C_{out}$$

Where $i_{aux}^{light-load}$ is the current drawn from auxiliary winding during light-load mode of operation (no switching) and $i_{sec}^{light-load}$ is the current drawn from the secondary side during light-load mode of operation (no switching).

Design Example – *Vcc and Bias winding capacitances* for a typical 65W USB-PD adapter

The VCC capacitance value is selected to be 15uF and a polymer electrolytic type is selected in order to support -40 deg C startup.

The auxiliary capacitor (C_{aux}^{top}) is calculated as :

$$C_{aux}^{top} > \frac{i_{aux}^{light-load}}{i_{sec}^{light-load}} \cdot \frac{N_{sec}}{N_{aux}} \cdot C_{out}$$

$$C_{aux}^{top} > \frac{5mA}{11mA} \cdot \frac{5T}{3 \cdot 11T} \cdot 1360uF = 94uF \rightarrow 100uF$$

R_{SNS} and RC Filter Selection

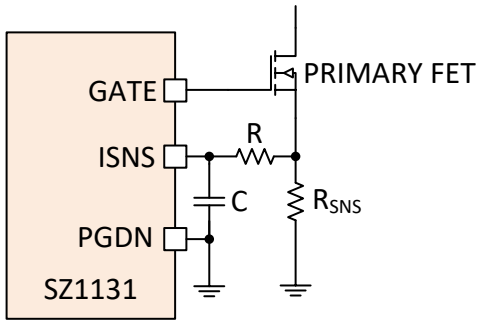

Figure 5: R_{SNS} and RC filter circuit

SZ1131 implements two different ISNS thresholds. The skip pulse current threshold (V_{ISNS_SKIP}) is enabled during the light load operating conditions to improve efficiency. The peak current limit threshold (V_{ISNS_PEAK}) protection is to ensure the transformer does not saturate beyond I_{max} value and also to implement over power protection (OPP).

The formula to calculate R_{SNS} is given by

$$R_{SNS} = \frac{V_{ISNS}^{PEAK}}{I_{MAX}}$$

where $V_{ISNS\_PEAK}^{MAX}$ is the typical maximum (lowest VBULK_S) peak-current sense limit, as defined in datasheet, equal to 285mV.

Design Example – *R_{sense}* for a typical 65W USB-PD adapter

$$R_{SNS} = \frac{285mV}{3.08A} = 92m\Omega$$

High frequency noise mitigation

To mitigate the effects of leading-edge current sensing noise, SZ1131 implements digital blanking, t_{ISNS_BLNK} (minimum value 221ns), of the current sensing comparator outputs. The main motivation is to ensure that the skip-pulse current limit (V_{ISNS_SKIP}) is enforced during light load mode of operation and that high-frequency noise does not cause reduced primary MOSFET on-time, which can negatively affect efficiency and BOOT_CL charging (AC FET ability to turn-on).

One example where additional RC filter between the R_{SNS} resistor and ISNS pin is necessary is shown in Figure 4.

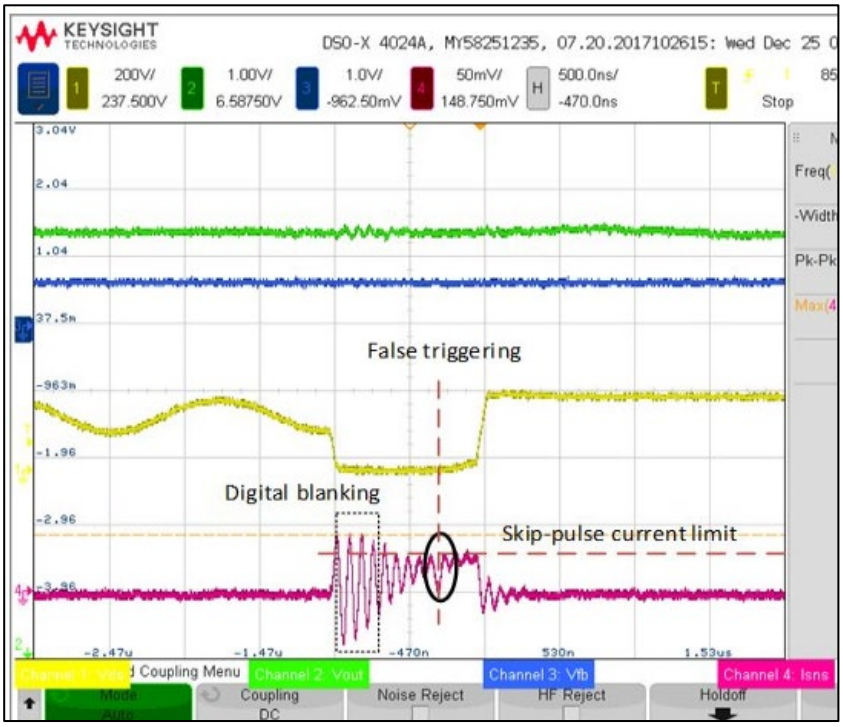

Figure 6: False triggering of skip-pulse current limit of due to high frequency noise

It should be noted that when a R_{SNS} RC filter is utilized it will result in higher skip-pulse and peak-current limits due to the added delay in detection. As a result, the peak-current limit value will increase by an amount equal to

$$i_{PCL}^{\Delta} = (1+\propto) \cdot \frac{BULK}{L_M} \cdot R \cdot C,$$

where α is given by

VBULK_S (DC)	α
<0.95V	0.75
≥0.95V, <1.7V	0.50
≥1.7V, < OVLO	0.375

Table 3: VBULK_S and corresponding α value

To maintain flat over-power protection, it is recommended that the RC filter be minimized to value less than 240ns (R = 10-24R and C = 10nF).

The skip-pulse current limit value will increase by an amount equal to

$$i_{SPL}^{\Delta} = \frac{BULK}{L_M} \cdot R \cdot C.$$

Minimization of output voltage ripple during light-load operation via reduction of SPL threshold

Certain applications may require <100mVpk-pk output voltage ripple during low output voltage and light-load operation. For these applications, this can be achieved by a reduction of the SPL threshold using the circuit shown in Figure 5.

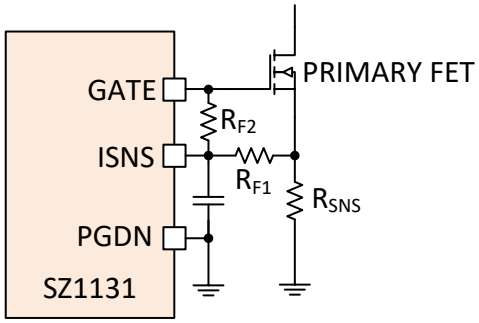

Figure 7: R_{SNS} and RC filter circuit

The SPL current reduction, as a relative ratio of SPL threshold, is given by equation

$$i_{SPL}^{\Delta ratio} = \frac{1}{1+\frac{R_{f2}}{R_{f1}}}.$$

Typical range of R_{f2} values that will ensure 70 to 80mV output voltage ripple during 5V output voltage operation are 16 to 20kΩ.

Configuration Resistor Selection (RCONFIG)

SZ1131 implements an innovative gate-driver composed of a programmable current source for controlled external switch turn-on and low resistance switch for fast external switch turn-off, as shown in Figure 6.

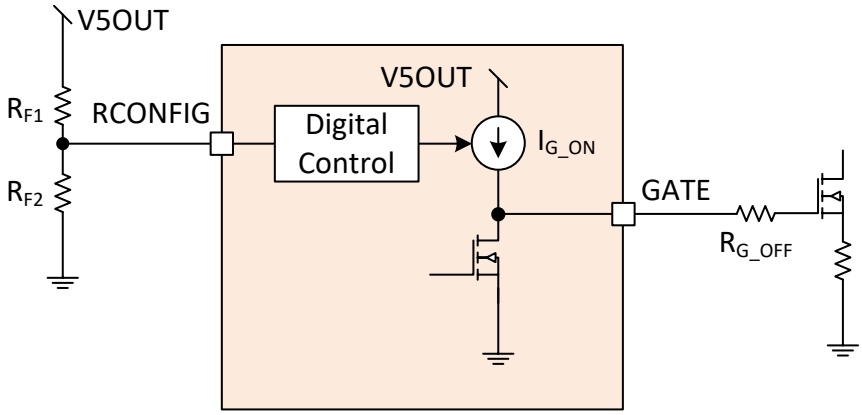

Figure 8: Hybrid gate-driver with current driven turn-on and low resistance switch turn-off

The turn-on current strength should be minimized in order to reduce the primary and secondary side switch drain-to-source slew rate during primary switch turn-on. In such a way, it may be possible to eliminate the voltage spike seen on the secondary side switch and enable for a) the use of lower breakdown voltage device, b) elimination of lossy snubber and c) improvement of third quadrant conducted EMI and first quadrant radiated EMI. Figure 7 illustrates the key primary and secondary side switch current and voltage waveforms for 8mA and 24mA driving strengths.

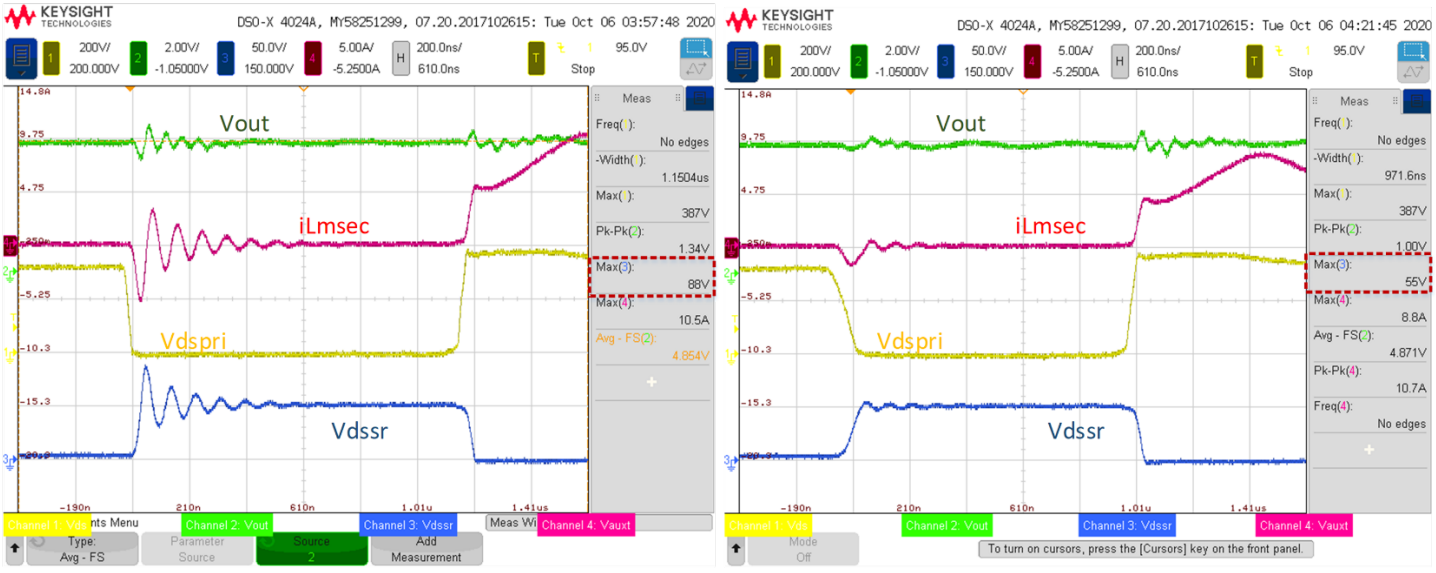

Figure 9: Secondary side MOSFET voltage and current waveforms with two turn-on drive strengths (24mA left and 8mA right) for 265Vac input voltage and 5V output voltage operating condition. The secondary side switch maximum voltage is reduced from 88V to 55V.

The key limitation in selecting the gate driver turn-on current strength is the effect on minimum effective primary switch on-time which is critical in order to ensure that the active clamp driver bootstrap capacitor can be charged sufficiently. The equation shown below can be used as a guide to determine the minimum required gate driver current strength in mA

$$I_{GATE}^{SRC} > \frac{C_{rss}^{@250V}}{100}$$

where C_{rss} is the primary MOSFET gate-to-drain capacitance at V_{DS}=250V in pF. Once the minimum drive strength required is determined the appropriate configuration would be selected via the configuration pull-up and pull-down resistors shown in the Table 4.

Configuration	$R_{PULL-UP}$ (R_{F1})	$R_{PULL-DOWN}$ (R_{F2})	Fault Recovery Behaviour	I_{GATE_SRC} (mA)
1	560	91	Latch	8
2	560	110		16
3	390	100		24
4	220	122	Hiccup (All Faults)	8
5	205	130		16
6	180	130		24
7	150	205	Hiccup with OTPs Latch	8
8	130	200		16
9	154	270		24

Table 4: Converter specification data

It should be noted that the primary switch turn-off time can be slowed down by addition of an external resistor RG_OFF between SZ1131 gate pin and the primary switch gate pin or by addition of drain-source capacitance (may be required for some types of primary devices).

If a cascode type of primary switch device is utilized (ie. Transphorm GaN devices) it is recommended that the lowest drive strength be utilized.

Design Example – *Configuration resistors* for a 65W USB-PD Adapter

The MOSFET chosen is Infineon IPP65R225C7. The minimum I_{GATE} can then be calculated as:

$$I_{GATE}^{SRC} > \frac{2.5}{100} = 25mA$$

The required gate-drive strength is 24mA and assuming that hiccup fault behaviour is desired the configuration resistors required would be:

$$R_{F1} = 180\ k\Omega$$

$$R_{F2} = 130\ k\Omega$$

Active Clamp Components (R_{CLAMP} and C_{CLAMP})

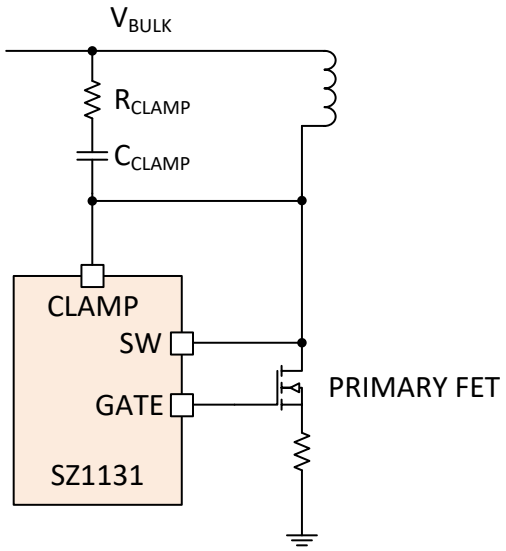

Figure 10: Clamp circuit consisting of active clamp capacitor, resistor and parallel diode.

The selection of the active clamp capacitor, C_{clamp}, is a two-step process. First, the initial estimation of C_{clamp} should be made based on the average transformer leakage inductance value, $L_{leakage}$, using the following equation.

$$C_{clamp} = \left(\frac{T_{RES}}{2\pi}\right)^2 \cdot \frac{1}{L_{leakage}}$$

Where, T_{RES} is the resonant period of C_{clamp} and $L_{leakage}$, which should be set to 1µs. If $L_{leakage}$ is unknown, a reasonable estimate would be 2% of the primary side magnetizing inductance.

Second, check T_{RES} during full-power operation, at maximum output voltage, and adjust C_{clamp} to ensure 0.9-1µs resonant period is achieved. Figure 10 identifies this resonant period from the drain voltage waveform of the primary FET after it turns off.

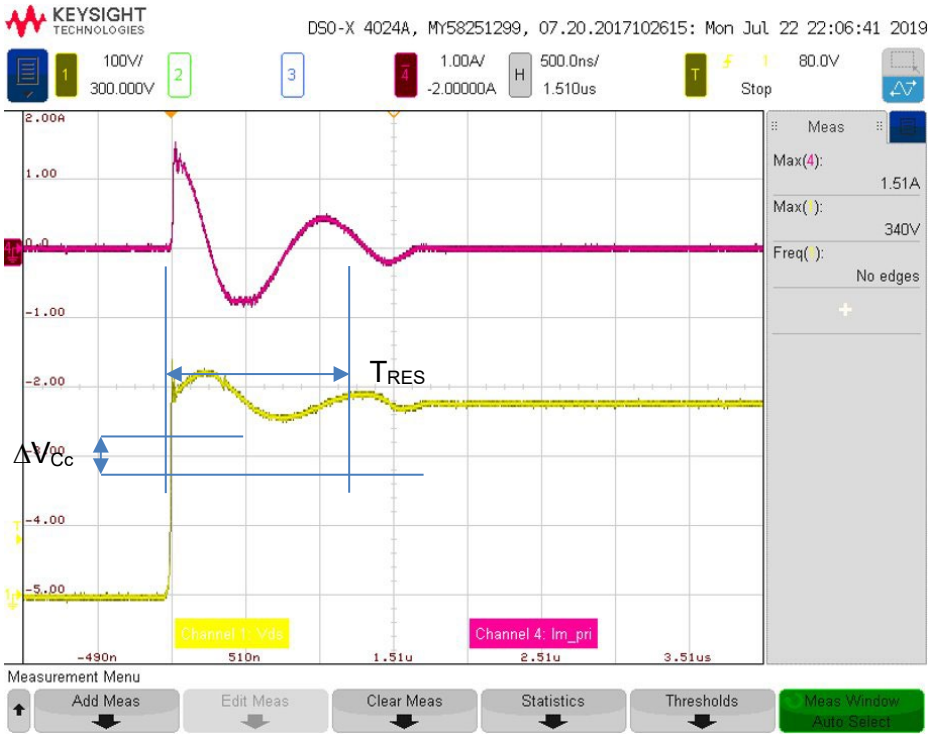

Figure 11: Typical primary MOSFET drain voltage and active clamp current with the active clamp resonant period highlighted

The voltage rating of C_{clamp} needs to be calculated to withstand the DC component of reflected output voltage and the AC component of ΔVC_{Clamp}:

$$V_{MIN\_C_C} = V_{OUT\_MAX} \cdot \frac{N_{PRI}}{N_{SEC}} + \Delta V_{C_C}$$

where the AC component ΔVCC, is given by:

$$\Delta V_{C_C} \approx \frac{\pi}{4} \cdot I_{max} \cdot \sqrt{\frac{L_{LK}}{C_C}}$$

$$= \frac{\pi}{4} \cdot 0.6 \cdot \frac{V_{ISNS\_PEAK}}{R_{SENSE}} \cdot \sqrt{\frac{L_{LK}}{C_C}}$$

It should be noted that the I_{max} current is lower than the peak current through the transformer since portion of the leakage energy is transferred to the effective capacitance from SW node to primary ground.

Design Example – *Clamp capacitor* for a typical 65W USB-PD adapter

For the primary magnetizing inductance of 250uH, considering leakage inductance to be ~2% and setting the resonant period as 1us.

Leakage inductance = 2% L_M = 5µH

Capacitor clamp,

$$C_{clamp} = \left(\frac{1.10^{-6}}{2\pi}\right)^2 \cdot \frac{1}{5 \cdot 10^{-6}.} = 5.1nF$$

the AC component ΔVCC,

$$\Delta V_{C_C} = \frac{0.6 \cdot \pi \cdot 285mV}{4 \cdot 90\text{m}\Omega} \cdot \sqrt{\frac{5\mu\text{H}}{5.1\text{nF}}} = 41.1V$$

Minimum voltage rating of the capacitor,

$$V_{MIN\_C_C} = 20V \cdot \frac{36\text{T}}{5\text{T}} + 41.1\text{V} = 185\text{V (250V)}$$

The optimal point to turn-on the AC FET is when active clamp current is flowing through the AC FET body diode (ZVS) and optimal point to turn-off is when active clamp current is close to zero (ZCS) or the AC FET body diode is conducting (ZVS). If the variation of the leakage inductance and clamp capacitor value (ex. C0G) can be controlled within 0.7-1.4x of nominal value a series clamp resistor is not required (ZVS will be achieved during turn on and turn off).

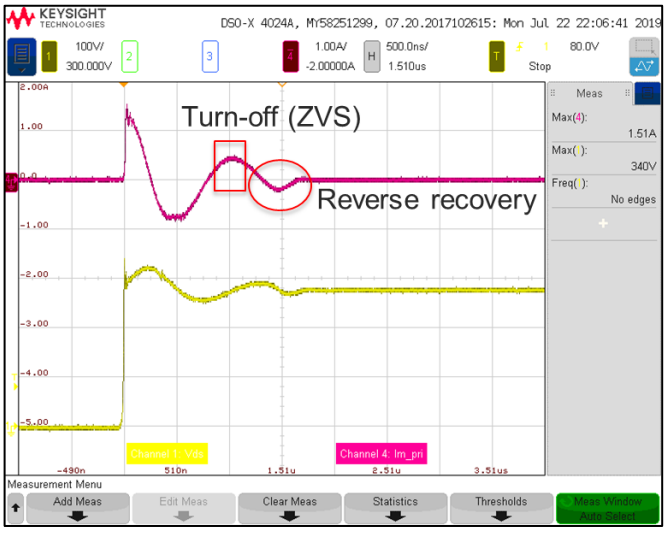

Figure 12: 115Vac/20V/3A w/o clamp resistor. CH1 is the primary MOSFET drain voltage and CH4 is the active clamp current (positive from source-to-drain).

If the leakage inductance cannot be well controlled (within 0.7-1.4x), it is recommended to add a clamp resistor in series, typically 10R (10R 1812 footprint, 20R 2512), to ensure the AC FET turn-off is soft-switched (ZCS).

Figure 12 illustrates the active clamp current without a clamp resistor (ZVS turn-on and turn-off) and Figure 13 illustrates the active clamp current with a 20R clamp resistor (ZVS turn-on and ZCS turn-off).

Figure 13: 115Vac/20V/3A w/ 20R clamp resistor. CH1 is the primary MOSFET drain voltage and CH4 is the active-clamp current (positive from source-to-drain).

Active Clamp Gate Drive Bootstrap (BOOT_CL)

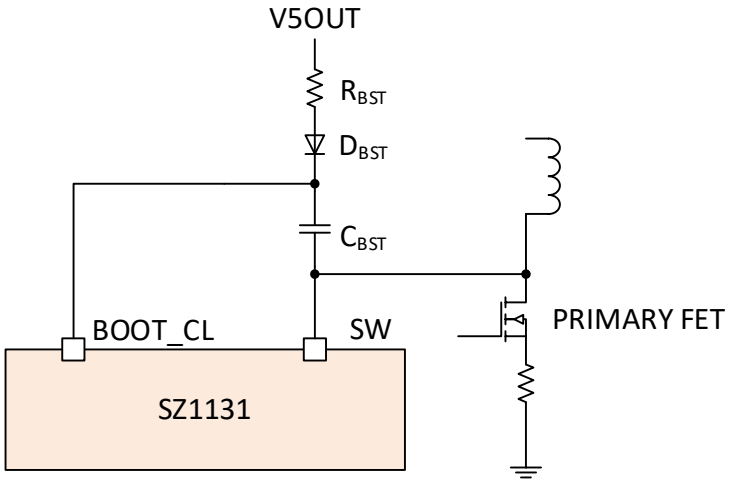

Figure 14: Bootstrap capacitor circuit

The voltage supply to the internal AC FET high side driver is provided by the C_{BST} connected between the BOOT_CL & SW pin. To ensure that AC FET is active, the C_{BST} must be sufficiently charged above AC FET driver UVLO, POR_{RISE_ADR} (3.74V max). This is achieved by utilizing a fast bootsrap diode and appropriately sized bootstrap capacitor. Furthermore, the BOOT_CL charging current must not trigger the current sense thresholds and as a result a 4.7R bootstrap diode series resistor is required.

Design Example – *BOOT_CL* recommended values for a typical 65W USB-PD adapter

Parameter	Value
C_{BST}	22nF (50V, X7R)
R_{BST}	4.7Ω
D_{BST}	US1MFA

BULK_S Resistors

The under-voltage/brown-out/brown-in are implemented using bulk capacitor voltage sensing with a resistor divider connected to V_{BULK_S}.

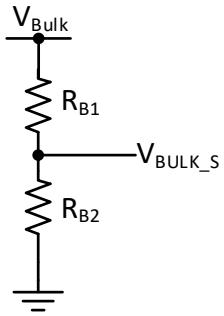

Figure 15: Simple bulk voltage sensing circuit

A basic resistor divider, as shown in Figure 14, can be utilized to ensure operation over universal line voltage range with margin. To minimize the no-load power a large R_{B1} resistance value, 4x22MΩ, is recommended.

The BULK_S pull-down resistance should be calculated taking into account the desired maximum brown-in voltage ($V_{AC}^{brown-in}$), the BULK_S brown-in threshold V_{UV_REC} (0.655V), and the desired R_{B1} resistance value. Both R_{B1} & R_{B2} are recommended to be within 1% tolerance.

$$R_{B2} = \frac{R_{B1}}{\left(\frac{V_{BULK}^{brown-in}}{V_{UV\_REC}} - 1\right)} = \frac{88M\Omega}{\frac{V_{AC}^{brown-in} \cdot \sqrt{2}}{0.655V} - 1}$$

Once R_{B1} and R_{B2} are calculated the minimum AC line OVLO voltage can be determined using the minimum BULK_S OVLO threshold V_{OVLO_TH} (2.09V) and the following equation:

$$V_{AC}^{OVLO} = \frac{1}{\sqrt{2}} \cdot V_{OVLO\_TH} \cdot \left(\frac{R_{B1}}{R_{B2}} + 1\right) = \frac{2.09V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{R_{B2}} + 1\right)$$

Furthermore, the minimum AC line OVLO recovery voltage can be determined using the minimum BULK_S recovery from over-voltage threshold V_{OVLO_REC} (2.05V) and the following equation:

$$V_{AC}^{OVLO\_Rec} = \frac{1}{\sqrt{2}} \cdot V_{OVLO\_REC} \cdot \left(\frac{R_{B1}}{R_{B2}} + 1\right) = \frac{2.05V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{R_{B2}} + 1\right)$$

Design Example – *BULK_S sensing resistors* for a typical USB-PD adapter with universal input

The desired maximum brown-in voltage is set to 87Vac to ensure sufficient margin for input AC line variations and BULK_S resistor divider ratio accuracy. For this application we wish to minimize no-load power; therefore, the BULK_S pull-up resistance is chosen to be 4x22M (88MΩ). Finally, the required pull-down resistance is calculated to be equal to

$$R_{B2} = \frac{88M\Omega}{\frac{87Vac \cdot \sqrt{2}}{0.655V} - 1} = 471k\Omega = 470\text{K}\Omega \text{ (standard value)}$$

Utilizing R_{B1} and R_{B2} the minimum AC OVLO and AC OVLO recovery voltages are calculated

$$\text{Minimum AC OVLO : } V_{AC}^{OVLO} = \frac{2.09V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{470k\Omega} + 1\right) = 278Vac$$

$$\text{Minimum AC OVLO recovery : } V_{AC}^{OVLO\_Rec} = \frac{2.05V}{\sqrt{2}} \cdot \left(\frac{88M\Omega}{470k\Omega} + 1\right) = 273Vac$$

For applications where the input to the active clamp flyback is coming off a front end PFC converter, care should be taken to ensure that the brown-in and brown-out levels are chosen according to the DC input provided by the front end boost converter.

VAUX_S Resistors

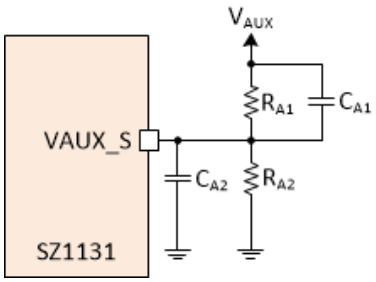

Figure 16: V_{AUX} voltage sense circuit

VAUX_S is the sensing pin for attenuated auxiliary voltage and is primarily utilized to support Quasi-Resonant (QR) mode of operation and determine when to turn-on the active clamp FET. An internal QR valley comparator, connected to V_{AUX_S}, detects the QR valley points. Furthermore, QR valley comparator is used to change the mode of operation from fixed frequency DCM to valley switching DCM during start-up and to provide output short circuit protection.

For sensing the reflected voltage on the auxiliary winding, a resistor divider is placed at the V_{AUX_S} pin (R_{A1} and R_{A2}).

$$V_{VAUX\_S} = \frac{R_{A2}}{R_{A1} + R_{A2}} \cdot V_{AUX}$$

The optimal divider ratio depends on the maximum output voltage levels of the AC/DC converter, as well as the transformer turns ratios. R_{A1} and R_{A2} resistors values should be chosen such that, under no operating conditions, V_{AUX_S} pin voltage exceeds the absolute maximum voltage rating (±8V).

$$V_{AUX\_S}^{MAX} = \left(V_{BULK\_MAX} \cdot \frac{N_{AUX}}{N_{PRI}}\right) \cdot \frac{R_{A2}}{R_{A1} + R_{A2}}$$

The lower resistor R_{A2} value should be selected considering potential pin-to-pin short condition between V_{AUX_S} and V_{BULK_S}. For such a fault case, it is desirable that V_{BULK_S} be pulled down below the SZ1131 BULK UVLO, V_{UV_TH} (258mV), for all expected input voltage operating conditions, such that SZ1131 remains in a non-switching state. Typical R_{A2} value required to ensure safe operation is 1/20th the value of BULK_S pull-down resistor R_{B2}. When calculating R_{A1} it is recommended to add ~10% safety margin to V_{BULK_MAX}.

It should be noted that a 0.5-1.5pF feedforward capacitor C_{A1} may need to be added in order to ensure accurate valley detection if valley switching is late. Furthermore, if the primary switch drain voltage is early (before the valley) or parasitic coupling is causing peaking of VAUX_S voltage a 15-68pF VAUX_S to PRGND capacitance C_{A2} may need to be added. The final circuit parameters should be confirmed experimentally by sensing VAUX_S and ensuring valley switching is accurate and VAUX_S voltage is within the pin absolute maximum rating.

Design Example - *VAUX_S resistors* for a typical 65W USB-PD adapter

R_{A2} value should be less than 470kΩ / 20 = 23.5kΩ, so 20k is chosen.

The R_{A1} value can be calculated as

$$V_{AUX\_S}^{MAX} = \left(V_{BULK\_MAX} \cdot \frac{N_{AUX}}{N_{PRI}}\right) \cdot \frac{R_{A2}}{R_{A1} + R_{A2}}$$

$$8 = \left(265\text{Vrms} \cdot \sqrt{2} \cdot 1.1 \cdot \frac{11T}{36T}\right) \cdot \frac{20\text{k}}{R_{A1} + 20\text{k}}$$

R_{A1} = 295k →300k (E24 value)

$$C_{A1} = 0\text{pF}$$

$$C_{A2} = 40\text{pF}$$

OTP NTC and Resistor

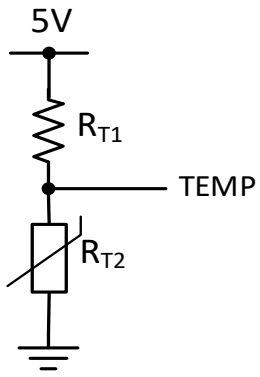

Figure 17: Over temperature sensing circuit

A second temperature monitor is provided by an external NTC (negative temperature coefficient) thermistor. The R_{T2} connected from TEMP pin to ground can be used to give over-temperature protection to the power supply from hotspots on the printed circuit board. At start-up, the voltage at TEMP needs to be higher than V_{NTCR} =1V for the IC to start operation. If the voltage at TEMP is lower than V_{NTCTH} = 0.61 after the start-up, the IC shuts down and recovery from shutdown takes place once the voltage is above 1V.

Once OTP set point and R_{T2} are determined the pull-up resistor R_{T1} can be determined using the minimum TEMP_S threshold V_{NTC_TH} (0.61V) and the following equation:

Design Example – *NTC selection* for a typical 65W USB-PD adapter

NCP15WL104E03RC (100k resistor at 25°C) is selected as the NTC resistor for the reference design. For a desired external OTP set point of 115°C R_{TI} pull up resistor is calculated as:

$$V_{NTC\_TH} = 5 \cdot \frac{R_{T2}^{120°C}}{R_{T1} + R_{T2}^{120°C}}$$

$$V_{NTC\_TH} = 5 \cdot \frac{R_{T2}^{115°C}}{R_{T1} + R_{T2}^{115°C}}$$

$$0.61V = 5V \cdot \frac{3.38\text{k}}{R_{T1} + 3.38\text{k}}$$

R_{TI} = 24.3k

OOVP_S Resistors

The OOVP_S pin senses the reflected output voltage through the auxiliary winding using a resistor divider circuit as shown in Figure 17. During each switching period output over-voltage protection is triggered if the reflected output voltage at pin OOVP_S exceeds V_{OOVP_TH} (1.4V).

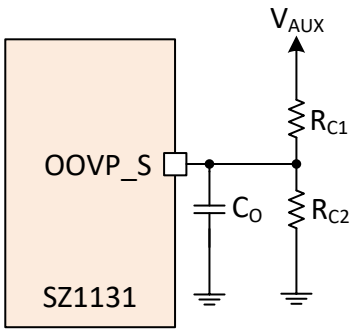

Figure 18: Resistor Divider for Output OVP Sensing

The following equation calculates the voltage at the OOVP_S pin for the earliest OOVP detection event

$$V_{OOVP\_S}^{min} = \frac{R_{C2}}{R_{C1}+R_{C2}} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \alpha \cdot V_{out}^{max} = V_{OOVP\_TH}^{min}$$

Where α is the multiplication factor of the nominal maximum output voltage for which the earliest OOVP will be detected (ie. 1.1 would be equivalent to 110% V_{out} limit for earliest OOVP), and V_{OOVP_TH} is minimum OOVP_S thresholds. A 15pF filtering capacitor is also recommended between OOVP_S and ground in order to attenuate any switching noise from coupling to the OOVP_S pin.

Design Example – *OOVP_S resistors* for a typical 65W USB-PD adapter

R_{C2} is selected to be 20k. With the output OOVP threshold set to 23V, R_{C1} can now be calculated using the equation,

$$V_{OOVP\_S}^{min} = \frac{R_{C2}}{R_{C1}+R_{C2}} \cdot \frac{N_{AUX}}{N_{SEC}} \cdot \alpha \cdot V_{out}^{max} = V_{OOVP\_TH}^{min}$$

$$2.28\text{V} = \frac{20k}{R_{C1}+20k} \cdot \frac{11T}{5T} \cdot 1.1 \cdot 20\text{V}$$

R_{C1} = 405kΩ

PCB layout considerations

Primary Loop Area

The loop consisting of the input bulk capacitor, primary switch and primary winding should be kept as small as possible. It is advised that these three components are in close proximity to minimize trace length between them.

Active Clamp Loop Area

The loop consisting of SZ1131 pin 1 (CLAMP), clamp resistors and capacitor, primary winding, and SZ1131 pin 3 (SW) should be kept as small as possible. It is a good practice to move this loop area outside of the primary loop area described in the previous section to prevent the clamp loop from occupying space within the primary loop area.

Secondary Loop Area

The secondary loop consisting of the secondary winding, output capacitors and synchronous rectifier should likewise be minimized. It is desirable to have these components near each other to minimize trace length.

Optimized Grounding

It is extremely useful to place a solid ground plane under the primary side flyback stage, as it will reduce conducted and radiated EMI. It is good practice to use a dedicated ground connection for power and small signal circuits of the power supply. Do not extend the ground plane to the area where the input filters are located as this will effectively bypass the EMI filters.

Bypass Capacitors

SZ1131 bypass capacitors should be placed directly across the pins to provide maximum decoupling.

EMI Filter PCB Placement

Ideally, the EMI filter section should be placed as far away from noise generating elements of the power supply to provide efficient filtering. This could be a challenge for high power density designs. As an alternative, it has been proven that using the bulk capacitor as a barrier between the filter section and the rest of the power supply can provide the same effect.

Y-Capacitor Connection

Termination of Y-capacitor should be between two electrically quiet nodes. Most common connections are between primary and secondary power grounds, output bus voltage node and/or bulk voltage node.

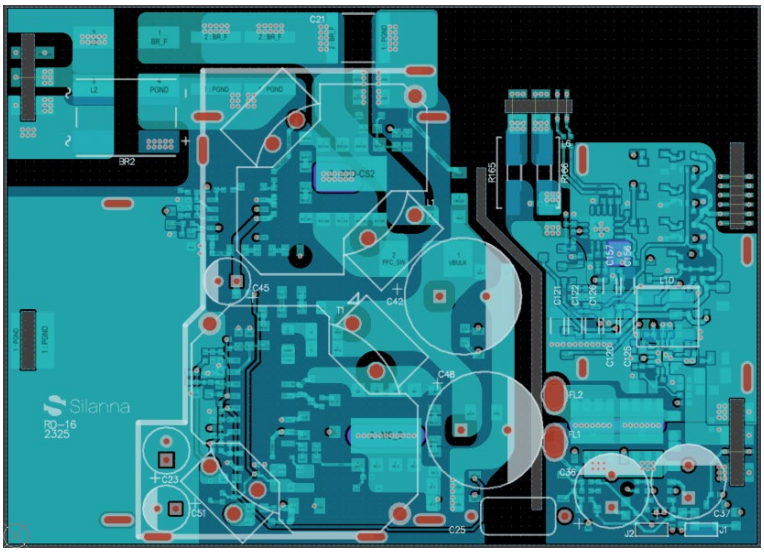

Figure 19: SZ1131 with optimized PCB layout.

EMI Design Considerations

Electromagnetic compatibility of a switchmode power supply is largely dictated by the switching actions of semiconductor devices, originating from the switching action of the primary switch. In the low frequency band (< 400kHz), differential mode noise relative to the fundamental switching frequency and its harmonics is dominant. For higher frequency band the common mode noise is dominant, mainly arising from fast semiconductor switching (voltage and current), circuit parasitics (capacitive and inductive coupling) as well as the magnetic fields of the power transformer. A wide variety of EMI filters and safety rated filter capacitors with different impedance characteristics are available to attenuate EMI and is commonly used in different power supplies. While most power supplies cannot go without filters, X-capacitors and Y-capacitors, these bring with them the consequences of higher dissipation losses, the added complexity in meeting safety regulations together with the added size and cost of the total solution.

Here are recommendations to significantly reduce EMI at its source to minimize the use of EMI mitigation components.

1. In the PCB layout stage take extra effort during component placement/selection to minimize parasitic coupling and provide knobs for potential tuning. Please refer to PCB layout guidelines in previous section.
2. The placement of snubbers across the synchronous rectifier and auxiliary diodes provide EMI reduction in the high frequency band of the conducted EMI spectrum as well as radiated EMI.
3. Standard recovery diodes usually have soft reverse recovery characteristics which is ideal in the reduction of conducted EMI in the high frequency range together with radiated EMI.
4. The slew rate of the primary switch drain node has a significant effect in high frequency EMI. A resistor placed in series with the gate of the switch can serves the purpose of reducing the slew rate. Care should be taken in the resistor selection since a very low slew rate may increase switching losses.
5. A small capacitor placed across the main switch will have the effect of reducing high frequency EMI. Limit the size of this capacitor as it will cause the dissipation on the primary switch to increase.
6. The transformer is a main contributor of common mode EMI. This can be significantly reduced by having the core electrically connected to ground and by using shield and cancellation windings. Please reach out to your nearest Silanna sales office for assistance in optimizing the shield winding configuration.

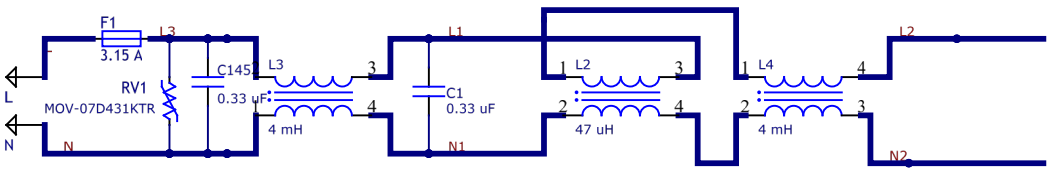

Figure 20: Typical front end filter of a 100W Adapter using SZ1131.

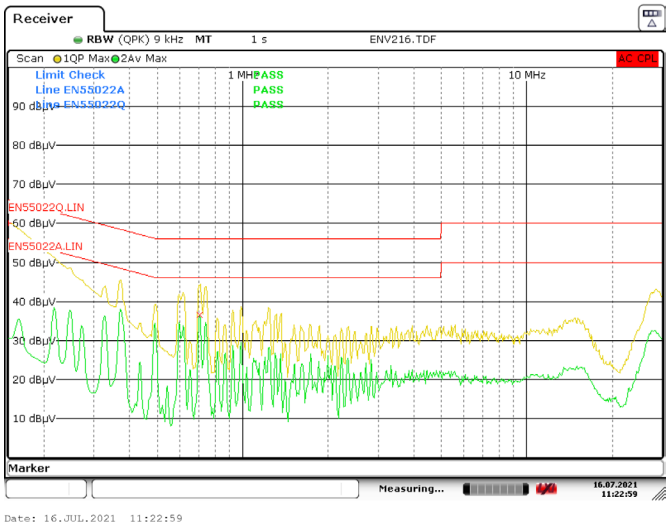

Figure 21: EMI of a 100W USB-PD Adapter using SZ1131following PCB and filter design recommendations.

Feedback Loop Design Considerations

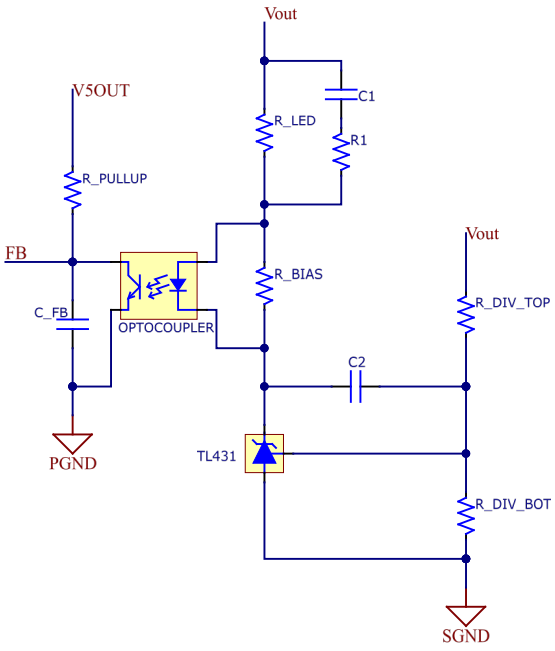

Figure 22: Typical feedback circuit using TL431 with a type 3 compensator

Selection of voltage divider resistors (R_div_top and R_div_bottom)

The top and bottom dividers together with the TL431 shunt regulator set the static output voltage regulation point. The resistor values are chosen according to this equation :

$$V_{out} = V_{ref} \frac{R_{div_{top}} + R_{div_{bot}}}{R_{div_{bot}}}$$

Where;

Vout = output voltage

Vref = TL431 reference voltage (2.495 V)

Rdiv_top = Top divider resistor

Rdiv_bot = Bottom resistor divider, usually set to 10 kohms

Optocoupler

With travel adapters and most modern power supplies, very low no load power consumption is desirable. For this reason, OPTO_LED driving current is often reduced to a few hundred microamperes. By doing this, an optocoupler's CTR can vary significantly which affects your actual cross over frequency. It is advised that take note of the minimum CTR values in designing the feedback network.

Biasing TL431

The TL431 requires a minimum current and a minimum voltage for it to maintain optimal operation. These set the maximum RLED value that can be used for a given design. This value can be determined using this equation :

$$R_{LED\_max} \leq \frac{V_{out} - V_f - V_{TL431\_min}}{V_{5out} - V_{CE_{sat}} + I_{bias} CTR_{min} R_{pullup}} . R_{pullup} CTR_{min}$$

Where :

Vout = Output voltage

Vf = LED forward voltage drop

VTL431_min = TL431 minimum anode to cathode voltage

V5out = pin 13 of SZ1131

VCEsat = optocoupler saturation voltage

IBIAS = TL431 bias current

CTRmin = mínimum current-transfer-ratio of optocoupler

Rpullup = Collector pull up resistor

Determining the transfer function of the power stage
The transfer function of a flyback converter operating in DCM is shown below :

$$P(s) = G_0 . \frac{1 + \frac{s}{\omega_{ESR}}}{1 + \frac{s}{\omega_P}}$$

Where G0 is the DC gain of the DCM flyback and is calculated as :

$$G_0 = \frac{V_o}{D} \; x \; \frac{N_s}{N_p}$$

Where:
VO = Output voltage
D = converter duty cycle
NS = Secondary turns
NP = Primary turns

ωP is the pole formed by the output load resistance and output capacitor

$$f_{P=} \frac{2}{2\pi \; x \; R_O x \; C_O}$$

and ωESR is the zero due to the output capacitor ESR

$$f_{ESR} = \frac{1}{2\pi \; x \; ESR \; x \; C_O}$$

Selection of crossover frequency
A common guideline in the selection of the crossover frequency is to place it below a tenth of the switching frequency. In most cases, this is enough to provide excellent transient response as well as noise immunity. It is advised to use a gain-phase analyzer together with the formulas in this application note in fine tuning the feedback response of the whole system.

Location of optocoupler pole

The optocoupler has an internal pole as a result of the parasitic capacitance in the collector and base of the OPTO_ BJT. The location of the optocoupler pole can be shifted by connecting a capacitor on the FB pin of SZ1131 .

The new pole location will now be :

$$f_p = \frac{1}{2\pi R_{pullup}(C_{fb} + C_{opto})}$$

Where :

Rpullup = Collector pull up resistor

Cfb = Capacitor connected across collector

COPTO = Collector-emitter capacitance

R_LED and R_bias

The choice of the optocoupler LED series resistor is dictated by the bias current requirement of the TL431 as well as the AC current which generates the error voltage on the optocoupler collector. R_LED together with R_pullup sets the midband gain of the transfer function.

The mid-band static gain is calculated as :

$$G_m = -\frac{R_{pullup}\,CTR}{R_{LED}+R_{bias}//R_d}\,\frac{R_{bias}}{R_{bias}+R_d}$$

Shown in Figure <x> is a type 3 compensator network. Location of poles and zeroes in a type 3 architecture are calculated as follows :

$$\omega_{Z1} = \frac{1}{R_{div\_top}C_2}$$

$$\omega_{Z2} = \frac{1}{(R_{LED}+R_1)C_1}$$

$$\omega_{P1} = \frac{1}{R_{pullup}C_{FB}}$$

$$\omega_{P2} = \frac{1}{R_1 C_1}$$

Shown in figure 23 is a TL431 based feedback circuit with typical component values. The diagram also shows Rsignal of 20 ohms which is the injection point of the error signal during gain-phase measurements.

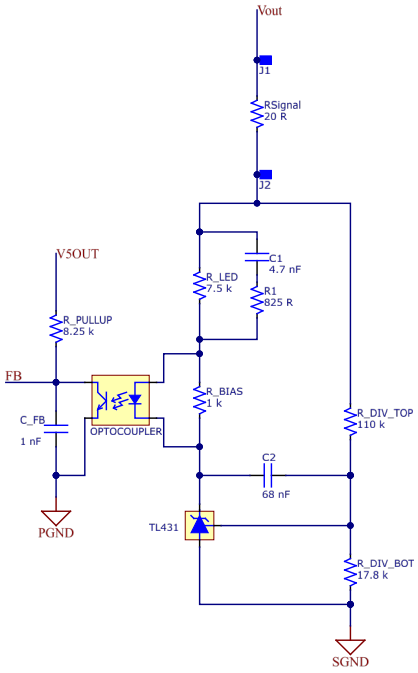

Figure 23:TL431 based feedback circuit with typical component values.

Version History

Date	Revision	Notes	Author
10/3/2023	1.0	Initial Release	Marketing Applications